Datasheet

AP5881

IEEE 802.11ax/ac/a/b/g/n 1x1

WiFi with Bluetooth5.2 Combo Sip Module

The revision history of the product specification

Version	Purpose	Date	Editor
1.0	Initial Doc	2023/1/5	Aaron

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CONTENTS

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1. Introduction

1.1 Product Overview

AP5881 is a fully Wi-Fi 6E and Bluetooth functionalities module with seamless roaming capabilities and advance security, also it can associate with different vendors' Wi-Fi 6E or legacy Access Points / Routers and run up to PHY rate of 600Mbps with single stream. Furthermore AP5881 included PCIe3.0 Gen2 and SDIO v3.0 and USB v2.0 alternative interface for Wi-Fi, UART/PCM/I2S interface for Bluetooth.

In addition, this compact module is a total solution for a combination of Wi-Fi + BT technologies. The module is specifically developed for tablet, OTT box and portable & mobile devices.

1.2 Product Features

1.2.1 WLAN

- Radio band support for 2.4 / 5 / 6 GHz band including 6GHz UNII-5,6,7,8.
- Support 802.11ax & legacy for 2.4 / 5 GHz band / 802.11ax only for 6GHz band.
- Single-stream spatial multiplexing up to 600 Mbps data rate.
- 20, 40, 80 MHz channels with optional SGI (1024 QAM modulation) for 5 / 6 GHz bands.
- Supports standard SDIO v3.0 and PCIe 3.0 Gen2, compatible with SDIO v2.0 HOST interfaces.
- TX and RX low-density parity check (LDPC) support for improved range and power efficiency

1.2.2 Bluetooth

- BT host digital interface:
  - HCI UART (up to 4 Mbps)
  - PCM for audio data
  - I2S Interface
- Complies with Bluetooth Core Specification Version 5.2 with provisions for supporting future specifications. With Bluetooth Class 1 or Class2 transmitter operation
- Supports extended synchronous connections (eSCO), for enhanced voice quality by allowing for retransmission of dropped packets
- Adaptive frequency hopping (AFH) for reducing radio frequency interference.

  A simplified block diagram of the module is depicted in the figure above d

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2. Specification

2.1 General Specification

Standards	IEEE 802.11 ax/ac/a/b/g/n 1T1R Wi-Fi + BT 5.2 Module Bluetooth V5.2, V5.0, V4.2, V4.1, V4.0 LE, V3.0+HS, V2.1+EDR
Chipset	Synaptics
Operating Frequency	2.400 GHz ~ 2.4835 GHz (2.4GHz ISM Band) 5.15~5.35GHz、5.47~5.725GHz、5.725~5.85GHz、5.955~6.415GHz 6.435~6.515GHz、6.535~6.855GHz、6.875~7.115GHz (5/6GHz UNII Band) Bluetooth: 2.402 GHz ~ 2.480 GHz
Modulation	WiFi: 802.11b: DSSS (DBPSK, DQPSK, CCK) 802.11g: OFDM (BPSK, QPSK, 16-QAM, 64-QAM) 802.11gn: OFDM (BPSK, QPSK, 16-QAM, 64-QAM) 802.11a: OFDM (BPSK, QPSK, 16-QAM, 64-QAM) 802.11an: OFDM (BPSK, QPSK, 16-QAM, 64-QAM) 802.11ac: OFDM (BPSK, QPSK, 16-QAM, 64-QAM, 256-QAM) 802.11ax: OFDMA (BPSK, QPSK, 16-QAM, 64-QAM, 256-QAM, 1024-QAM) BT: Header: GFSK Payload 2M: π/4-DQPSK Payload 3M: 8-DPSK
Interface	WLAN: SDIO V3.0/2.0 and PCIe 3.0 Gen2 and USB2.0 Bluetooth: UART / PCM / I2S
Form Factor	SiP (System in Package) Stamp Type
Antenna	External
Dimension	L x W x H: 8.5 x 8.5 (typical) mm x 1.0mm(Max.)
Operating temperature	-30°C~85°C
Storage temperature	-40°C~125°C
Humidity (Non-Condensing)	10%~ 95% (Operating)
Weight	0.40g
Driver Support	Linux, Android

Note: The optimal RF performance specified in the data sheet, however, is guaranteed only -10 °C to +55 °C and 3.2V < VBAT < 3.8V without derating performance.

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2.2 WiFi 2.4GHz RF Specification

Conditions: VBAT=3.3V; VDDIO=1.8V; Temp:25℃

Output Power, tolerance ± 1.5dB **The transmit EVM quality & spectrum mask are compliant with IEEE 802.11 standard**						
802.11b	1Mbps	2Mbps	5.5Mbps	11Mbps		
	17	17	17	17		
802.11g	6、9Mbps	12、18Mbps	24Mbps	36Mbps	48Mbps	
	17	17	16	16	15	
	54Mbps					
	15					
802.11n 20MHz	MCS0~2	MCS3	MCS4	MCS5	MCS6	
	17	17	16	16	15	
	MCS7					
	15					
802.11ax 20MHz	HE0~2	HE3	HE4	HE5	HE6	
	17	17	16	16	15	
	HE7	HE8	HE9			
	15	14	13			

802.11ax_20MHz SISO	Data rate	Tones	Spec(dBm)	Data rate	Tones	Spec(dBm)
	HE0	26	17	HE6	26	15
		52	17		52	15
		106	17		106	15
		242	17		242	15
	HE1-2	26	17	HE7	26	15
		52	17		52	15
		106	17		106	15
		242	17		242	15
	HE3	26	17	HE8	26	14
		52	17		52	14
		106	17		106	14
		242	17		242	14
	HE4	26	16	HE9	26	13
		52	16		52	13
		106	16		106	13
		242	16		242	13
	HE5	26	16			
		52	16			
		106	16			
		242	16			

Note: The specifications of RF output power are subject to change to fulfill the safety regulation and requirements in end-user product.

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Sensitivity, tolerance ± 2 dB CCK modulation PER ≦ 8%、OFDM modulation PER ≦ 10%				
802.11b	Data Rate	Spec.(dBm)		
	1Mbps	-96		
	2Mbps	-90		
	5.5Mbps	-88		
	11Mbps	-87		
802.11g	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	6Mbps	-91	24Mbps	-83
	9Mbps	-88	36Mbps	-80
	12Mbps	-87	48Mbps	-76
	18Mbps	-85	54Mbps	-73
802.11n_20MHz	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	MCS0	-90	MCS4	-77
	MCS1	-85	MCS5	-75
	MCS2	-84	MCS6	-72
	MCS3	-80	MCS7	-71
802.11ax_20MHz	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	HE0	-90	HE6	-72
	HE1	-85	HE7	-71
	HE2	-84	HE8	-69
	HE3	-80	HE9	-68
	HE4	-77		
	HE5	-75		
Maximum Input Level	802.11b: -10 dBm			
	802.11g/n/ax: -20 dBm			

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2.3 WiFi 5GHz RF Specification

Conditions: VBAT=3.3V ; VDDIO=1.8V ; Temp:25°C

Output Power, tolerance ± 2 dB **The transmit EVM quality & spectrum mask are compliant with IEEE 802.11 standard**					
802.11a	Frequency (MHz)	6~9Mbps	12~18Mbps	24Mbps	36Mbps
	5150~5350	16	16	16	16
	5470~5720	16	16	16	16
	5725~5845	16	16	16	16
	Frequency (MHz)	48Mbps	54Mbps		
	5150~5350	16	15		
	5470~5720	16	15		
	5725~5845	16	15		
802.11n 20MHz	Frequency (MHz)	MCS0~2	MCS3	MCS4	MCS5
	5150~5350	16	16	16	16
	5470~5720	16	16	16	16
	5725~5845	16	16	16	16
	Frequency (MHz)	MCS6	MCS7		
	5150~5350	15	14.5		
	5470~5720	15	14.5		
	5725~5845	15	14		
802.11n 40MHz	Frequency (MHz)	MCS0~2	MCS3	MCS4	MCS5
	5150~5350	15.5	15.5	15.5	15.5
	5470~5720	15.5	15.5	15.5	15.5
	5725~5845	15.5	15.5	15.5	15.5
	Frequency (MHz)	MCS6	MCS7		
	5150~5350	15	14		
	5470~5720	15	14		
	5725~5845	15	14		
802.11ac 20MHz	Frequency (MHz)	MCS0~2	MCS3	MCS4	MCS5
	5150~5350	16	16	16	16
	5470~5720	16	16	16	16
	5725~5845	16	16	16	16
	Frequency (MHz)	MCS6	MCS7	MCS8	
	5150~5350	15	14.5	12.5	
	5470~5720	15	14.5	12.5	
	5725~5845	15	14.5	12.5	

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802.11ac 40MHz	Frequency (MHz)	MCS0~2	MCS3	MCS4	MCS5
	5150~5350	15.5	15.5	15.5	15.5
	5470~5720	15.5	15.5	15.5	15.5
	5725~5845	15.5	15.5	15.5	15.5
	Frequency (MHz)	MCS6	MCS7	MCS8	MCS9
	5150~5350	15	14	12.5	11
	5470~5720	15	14	12.5	11
	5725~5845	15	14	12.5	11
802.11ac 80MHz	Frequency (MHz)	MCS0~2	MCS3	MCS4	MCS5
	5150~5350	15.5	15.5	15.5	15.5
	5470~5720	15.5	15.5	15.5	15.5
	5725~5845	15.5	15.5	15.5	15.5
	Frequency (MHz)	MCS6	MCS7	MCS8	MCS9
	5150~5350	15	14	12.5	11
	5470~5720	15	14	12.5	11
	5725~5845	15	14	12.5	11
802.11ax 20MHz	Frequency (MHz)	HE0~2	HE3	HE4	HE5
	5150~5350	16	16	16	16
	5470~5720	16	16	16	16
	5725~5845	16	16	16	16
	Frequency (MHz)	HE6	HE7	HE8	HES9
	5150~5350	15	14	12.5	11
	5470~5720	15	14	12.5	11
	5725~5845	15	14	12.5	11
	Frequency (MHz)	HE10	HE11		
	5150~5350	10	10		
	5470~5720	10	10		
	5725~5845	10	10		
802.11ax 40MHz	Frequency (MHz)	HE0~2	HE3	HE4	HE5
	5150~5350	15.5	15.5	15.5	15.5
	5470~5720	15.5	15.5	15.5	15.5
	5725~5845	15.5	15.5	15.5	15.5
	Frequency (MHz)	HE6	HE7	HE8	HES9
	5150~5350	15	14	12.5	11
	5470~5720	15	14	12.5	11
	5725~5845	15	14	12.5	11
	Frequency (MHz)	HE10	HE11		
	5150~5350	10	10		
	5470~5720	10	10		
	5725~5845	10	10		

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802.11ax 80MHz	Frequency (MHz)	HE0~2	HE3	HE4	HE5
	5150~5350	15.5	15.5	15.5	15.5
	5470~5720	15.5	15.5	15.5	15.5
	5725~5845	15.5	15.5	15.5	15.5
	Frequency (MHz)	HE6	HE7	HE8	HES9
	5150~5350	15	14	12.5	11
	5470~5720	15	14	12.5	11
	5725~5845	15	14	12.5	11
	Frequency (MHz)	HE10	HE11		
	5150~5350	9	9		
	5470~5720	9	9		
	5725~5845	9	9		
Note: The specifications of RF output power are subject to change to fulfill the safety regulation and requirements in end-user product.					

	Dara rate	Tones	Frequency	Spec.(dBm)
802.11ax_20MHz	HE0~2	26	5150~5350	16
			5470~5720	16
			5725~5845	16
		52	5150~5350	16
			5470~5720	16
			5725~5845	16
		106	5150~5350	16
			5470~5720	16
			5725~5845	16
		242	5150~5350	16
			5470~5720	16
			5725~5845	16
	HE3~4	26	5150~5350	16
			5470~5720	16
			5725~5845	16
		52	5150~5350	16
			5470~5720	16
			5725~5845	16
		106	5150~5350	16
			5470~5720	16
			5725~5845	16
		242	5150~5350	16
			5470~5720	16
			5725~5845	16

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802.11ax_20MHz	HE5~7	26	5150~5350	14
			5470~5720	14
			5725~5845	14
		52	5150~5350	14
			5470~5720	14
			5725~5845	14
		106	5150~5350	14
			5470~5720	14
			5725~5845	14
		242	5150~5350	14
			5470~5720	14
			5725~5845	14
	HE8~9	26	5150~5350	11
			5470~5720	11
			5725~5845	11
		52	5150~5350	11
			5470~5720	11
			5725~5845	11
		106	5150~5350	11
			5470~5720	11
			5725~5845	11
		242	5150~5350	11
			5470~5720	11
			5725~5845	11
	HE10~11	242	5150~5350	10
			5470~5720	10
			5725~5845	10

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	Dara rate	Tones	Frequency	Spec.(dBm)
802.11ax_40MHz	HE0~2	26	5150~5350	15.5
			5470~5720	15.5
			5725~5845	15.5
		52	5150~5350	15.5
			5470~5720	15.5
			5725~5845	15.5
		106	5150~5350	15.5
			5470~5720	15.5
			5725~5845	15.5
		242	5150~5350	15.5
			5470~5720	15.5
			5725~5845	15.5
		484	5150~5350	15.5
			5470~5720	15.5
			5725~5845	15.5
	HE3~4	26	5150~5350	15.5
			5470~5720	15.5
			5725~5845	15.5
		52	5150~5350	15.5
			5470~5720	15.5
			5725~5845	15.5
		106	5150~5350	15.5
			5470~5720	15.5
			5725~5845	15.5
		242	5150~5350	15.5
			5470~5720	15.5
			5725~5845	15.5
		484	5150~5350	15.5
			5470~5720	15.5
			5725~5845	15.5

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	Dara rate	Tones	Frequency	Spec.(dBm)
802.11ax_40MHz	HE5~7	26	5150~5350	14
			5470~5720	14
			5725~5845	14
		52	5150~5350	14
			5470~5720	14
			5725~5845	14
		106	5150~5350	14
			5470~5720	14
			5725~5845	14
		242	5150~5350	14
			5470~5720	14
			5725~5845	14
		484	5150~5350	14
			5470~5720	14
			5725~5845	14
	HE8~9	26	5150~5350	11
			5470~5720	11
			5725~5845	11
		52	5150~5350	11
			5470~5720	11
			5725~5845	11
		106	5150~5350	11
			5470~5720	11
			5725~5845	11
		242	5150~5350	11
			5470~5720	11
			5725~5845	11
		484	5150~5350	11
			5470~5720	11
			5725~5845	11
	HE10~11	242	5150~5350	10
			5470~5720	10
			5725~5845	10
		484	5150~5350	10
			5470~5720	10
			5725~5845	10

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	Dara rate	Tones	Frequency	Spec.(dBm)
802.11ax_80MHz	HE0~2	26	5150~5350	15.5
			5470~5720	15.5
			5725~5845	15.5
		52	5150~5350	15.5
			5470~5720	15.5
			5725~5845	15.5
		106	5150~5350	15.5
			5470~5720	15.5
			5725~5845	15.5
		242	5150~5350	15.5
			5470~5720	15.5
			5725~5845	15.5
		484	5150~5350	15.5
			5470~5720	15.5
			5725~5845	15.5
		996	5150~5350	15.5
			5470~5720	15.5
			5725~5845	15.5
	HE1~2	26	5150~5350	15.5
			5470~5720	15.5
			5725~5845	15.5
		52	5150~5350	15.5
			5470~5720	15.5
			5725~5845	15.5
		106	5150~5350	15.5
			5470~5720	15.5
			5725~5845	15.5
		242	5150~5350	15.5
			5470~5720	15.5
			5725~5845	15.5
		484	5150~5350	15.5
			5470~5720	15.5
			5725~5845	15.5
		996	5150~5350	15.5
			5470~5720	15.5
			5725~5845	15.5

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	Dara rate	Tones	Frequency	Spec.(dBm)
802.11ax_80MHz	HE3~4	26	5150~5350	15.5
			5470~5720	15.5
			5725~5845	15.5
		52	5150~5350	15.5
			5470~5720	15.5
			5725~5845	15.5
		106	5150~5350	15.5
			5470~5720	15.5
			5725~5845	15.5
		242	5150~5350	15.5
			5470~5720	15.5
			5725~5845	15.5
		484	5150~5350	15.5
			5470~5720	15.5
			5725~5845	15.5
		996	5150~5350	15.5
			5470~5720	15.5
			5725~5845	15.5
	HE5~7	26	5150~5350	14
			5470~5720	14
			5725~5845	14
		52	5150~5350	14
			5470~5720	14
			5725~5845	14
		106	5150~5350	14
			5470~5720	14
			5725~5845	14
		242	5150~5350	14
			5470~5720	14
			5725~5845	14
		484	5150~5350	14
			5470~5720	14
			5725~5845	14
		996	5150~5350	14
			5470~5720	14
			5725~5845	14

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	Dara rate	Tones	Frequency	Spec.(dBm)
802.11ax_80MHz	HE8~9	26	5150~5350	11
			5470~5720	11
			5725~5845	11
		52	5150~5350	11
			5470~5720	11
			5725~5845	11
		106	5150~5350	11
			5470~5720	11
			5725~5845	11
		242	5150~5350	11
			5470~5720	11
			5725~5845	11
		484	5150~5350	11
			5470~5720	11
			5725~5845	11
		996	5150~5350	11
			5470~5720	11
			5725~5845	11
	HE10~11	242	5150~5350	9
			5470~5720	9
			5725~5845	9
		484	5150~5350	9
			5470~5720	9
			5725~5845	9
		996	5150~5350	9
			5470~5720	9
			5725~5845	9

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Sensitivity, tolerance ± 1.5 dB CCK modulation PER ≦ 8%、OFDM modulation PER ≦ 10%				
802.11a	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	6Mbps	-90	24Mbps	-83
	9Mbps	-90	36Mbps	-80
	12Mbps	-88	48Mbps	-75
	18Mbps	-86	54Mbps	-73
802.11n_20MHz	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	6Mbps	-90	24Mbps	-79
	9Mbps	-88	36Mbps	-76
	12Mbps	-86	48Mbps	-73
	18Mbps	-83	54Mbps	-72
802.11n_40MHz	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	MCS0	-88	MCS4	-77
	MCS1	-86	MCS5	-72
	MCS2	-83	MCS6	-70
	MCS3	-80	MCS7	-69
802.11ac_20MHz	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	MCS0	-90	MCS5	-75
	MCS1	-88	MCS6	-73
	MCS2	-86	MCS7	-70
	MCS3	-83	MCS8	-68
	MCS4	-79		
802.11ac_40MHz	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	MCS0	-88	MCS5	-72
	MCS1	-86	MCS6	-70
	MCS2	-83	MCS7	-69
	MCS3	-80	MCS8	-65
	MCS4	-76	MCS9	-64
802.11ac_80MHz	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	MCS0	-85	MCS5	-68
	MCS1	-82	MCS6	-67
	MCS2	-79	MCS7	-65
	MCS3	-76	MCS8	-62
	MCS4	-73	MCS9	-61

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802.11ax_20MHz	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	HE0	-90	HE6	-73
	HE1	-88	HE7	-70
	HE2	-86	HE8	-68
	HE3	-83	HE9	-64
	HE4	-79	HE10	-59
	HE5	-75	HE11	-57
802.11ax_40MHz	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	HE0	-88	HE6	-70
	HE1	-86	HE7	-69
	HE2	-83	HE8	-65
	HE3	-80	HE9	-64
	HE4	-76	HE10	-60
	HE5	-72	HE11	-55
802.11ax_80MHz	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	HE0	-85	HE6	-67
	HE1	-82	HE7	-65
	HE2	-79	HE8	-62
	HE3	-76	HE9	-61
	HE4	-73	HE10	-57
	HE5	-68	HE11	-53
Maximum Input Level	802.11a/n/ac/ax : -30 dBm			

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2.4 WiFi 6GHz RF Specification

Conditions: VBAT=3.3V ; VDDIO=1.8V ; Temp:25°C

Output Power, tolerance ± 2 dB **The transmit EVM quality & spectrum mask are compliant with IEEE 802.11 standard**					
802.11ax 20MHz	Frequency (MHz)	HE0~2	HE3	HE4	HE5
	5955~6415	15.5	15.5	15.5	15.5
	6435~6515	15.5	15.5	15.5	15.5
	6535~6855	15	15	15	15
	6875~7115	15	15	15	15
	Frequency (MHz)	HE6	HE7	HE8	HE9
	5955~6415	14.5	13.5	12	10.5
	6435~6515	14.5	13.5	12	10.5
	6535~6855	14	13	12.5	10
	6875~7115	14	13	12.5	10
	Frequency (MHz)	HE10	HE11		
	5955~6415	9.5	9.5		
	6435~6515	9.5	9.5		
	6535~6855	9	9		
	6875~7115	9	9		
802.11ax 40MHz	Frequency (MHz)	HE0~2	HE3	HE4	HE5
	5955~6415	15.5	15.5	15.5	15.5
	6435~6515	15.5	15.5	15.5	15.5
	6535~6855	15	15	15	15
	6875~7115	15	15	15	15
	Frequency (MHz)	HE6	HE7	HE8	HE9
	5955~6415	14.5	13.5	12	10.5
	6435~6515	14.5	13.5	12	10.5
	6535~6855	14	13	12.5	10
	6875~7115	14	13	12.5	10
	Frequency (MHz)	HE10	HE11		
	5955~6415	9.5	9.5		
	6435~6515	9.5	9.5		
	6535~6855	9	9		
	6875~7115	9	9		

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802.11ax 80MHz	Frequency (MHz)	HE0~2	HE3	HE4	HE5
	5955~6415	15	15	15	15
	6435~6515	15	15	15	15
	6535~6855	14.5	14.5	14.5	14.5
	6875~7115	14.5	14.5	14.5	14.5
	Frequency (MHz)	HE6	HE7	HE8	HE9
	5955~6415	14.5	13.5	12	10.5
	6435~6515	14.5	13.5	12	10.5
	6535~6855	14	13	12.5	10
	6875~7115	14	13	12.5	10
	Frequency (MHz)	HE10	HE11		
	5955~6415	8.5	8.5		
	6435~6515	8.5	8.5		
	6535~6855	8	8		
	6875~7115	8	8		
Note: The specifications of RF output power are subject to change to fulfill the safety regulation and requirements in end-user product.					

Sensitivity, tolerance ± 2 dB, OFDM modulation PER ≦ 10%				
802.11ax_20MHz SISO	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	HE0	-88	HE6	-71
	HE1	-86	HE7	-68
	HE2	-84	HE8	-66
	HE3	-83	HE9	-62
	HE4	-77	HE10	-57
	HE5	-73	HE11	-55
802.11ax_20MHz MIMO	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	HE0	-88	HE6	-71
	HE1	-86	HE7	-68
	HE2	-84	HE8	-66
	HE3	-81	HE9	-62
	HE4	-77	HE10	-57
	HE5	-73	HE11	-54

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802.11ax_40MHz SISO	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	HE0	-86	HE6	-68
	HE1	-84	HE7	-67
	HE2	-81	HE8	-63
	HE3	-78	HE9	-62
	HE4	-74	HE10	-68
	HE5	-70	HE11	-53
802.11ax_40MHz MIMO	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	HE0	-85	HE6	-68
	HE1	-84	HE7	-67
	HE2	-81	HE8	-63
	HE3	-78	HE9	-62
	HE4	-74	HE10	-58
	HE5	-70	HE11	-53
802.11ax_80MHz SISO	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	HE0	-83	HE6	-65
	HE1	-80	HE7	-63
	HE2	-77	HE8	-60
	HE3	-74	HE9	-59
	HE4	-71	HE10	-55
	HE5	-66	HE11	-51
802.11ax_80MHz MIMO	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	HE0	-82	HE6	-65
	HE1	-80	HE7	-63
	HE2	-77	HE8	-60
	HE3	-74	HE9	-59
	HE4	-71	HE10	-55
	HE5	-66	HE11	-50
Maximum Input Level	802.11g/n/ax: -30 dBm			

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2.5 Bluetooth RF Specification

Conditions: VBAT=3.3V ; VDDIO=1.8V ; Temp:25℃

RF Specification	
Output Power , tolerance ± 1.5 dB	
	CL1 (dBm)
BDR Output Power	16
EDR Output Power	9
BLE Output Power	16
Sensitivity, tolerance ± 1.5 dB	
Sensitivity @ BER=0.1% for GFSK (1Mbps)	-87 dBm
Sensitivity @ BER=0.01% for π/4-DQPSK (2Mbps)	-87 dBm
Sensitivity @ BER=0.01% for 8DPSK (3Mbps)	-84 dBm
Sensitivity @ BER=30.8% for LE (1Mbps)	-90 dBm
Sensitivity @ BER=30.8% for 2LE (2Mbps)	-90 dBm
Maximum Input Level	GFSK (1Mbps): -20dBm
	π/4-DQPSK (2Mbps): -20dBm
	8DPSK (3Mbps): -20dBm

Note*：The Bluetooth BDR output power is able to be configured by firmware (hcd file).

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3. Electrical Characteristics

3.1 Absolute Maximum Ratings

Symbol	Description	Min.	Max.	Unit
VBAT	Input supply Voltage	3.0	5.25	V
VDDIO	Digital/Bluetooth/SDIO/ I/O Voltage	1.62	1.95	V

Note : RF performance is optimal for 3.2V ≤ VBAT ≤ 5.0V. For 2.5 V≤VBAT ≤3.2V, device radios will operate but RF performance will degrade.

3.2 Recommended Operating Rating

The module requires two power supplies: VBAT and VDDIO.

Voltage rails	Min.	Typ.	Max.	Unit
VBAT	3.2	3.3	3.8	V
VDDIO	1.62	1.8	1.98	V

VBAT current consumption 1200mA(Peak), when VBAT = 3.3V

The module requires two power supplies: other Digital I/O Pins.

For VDDIO=1.8V	Min.	Max.	Unit
Input high voltage	0.65 x VDDIO	NA	V
Input low voltage	NA	0.35 x VDDIO	V
Output high voltage @ 2mA	VDDIO – 0.4	NA	V
Output low voltage @ 2mA	NA	0.4	V

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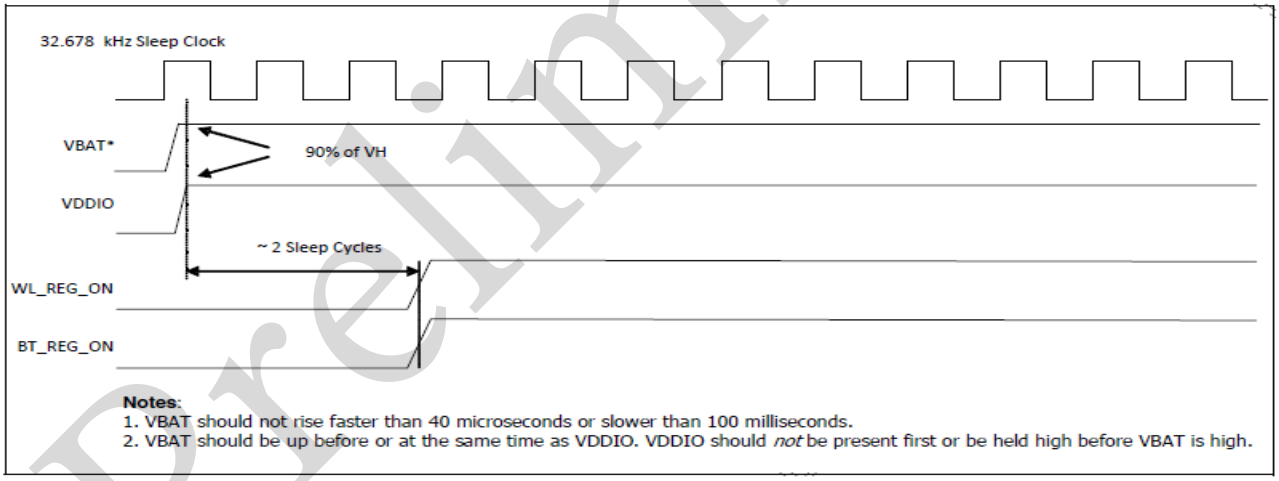
4. Host Interface Timing Diagram

4.1 Power-up Sequence Timing Diagram

The module has signals that allow the host to control power consumption by enabling or disabling the Bluetooth, WLAN and internal regulator blocks. These signals are described below. Additionally, diagrams are provided to indicate proper sequencing of the signals for carious operating states. The timing value indicated are minimum required values: longer delays are also acceptable.

- WL_REG_ON: Used by the PMU to power up or power down the internal regulators used by the WLAN section. When this pin is high, the regulators are enabled and the WLAN section is out of reset. When this pin is low the WLAN section is in reset.
- BT_REG_ON: Used by the PMU to power up or power down the internal regulators used by the BT section. Low asserting reset for Bluetooth. This pin has no effect on WLAN and does not control any PMU functions. This pin must be driven high or low (not left floating).



WLAN=ON, Bluetooth=ON

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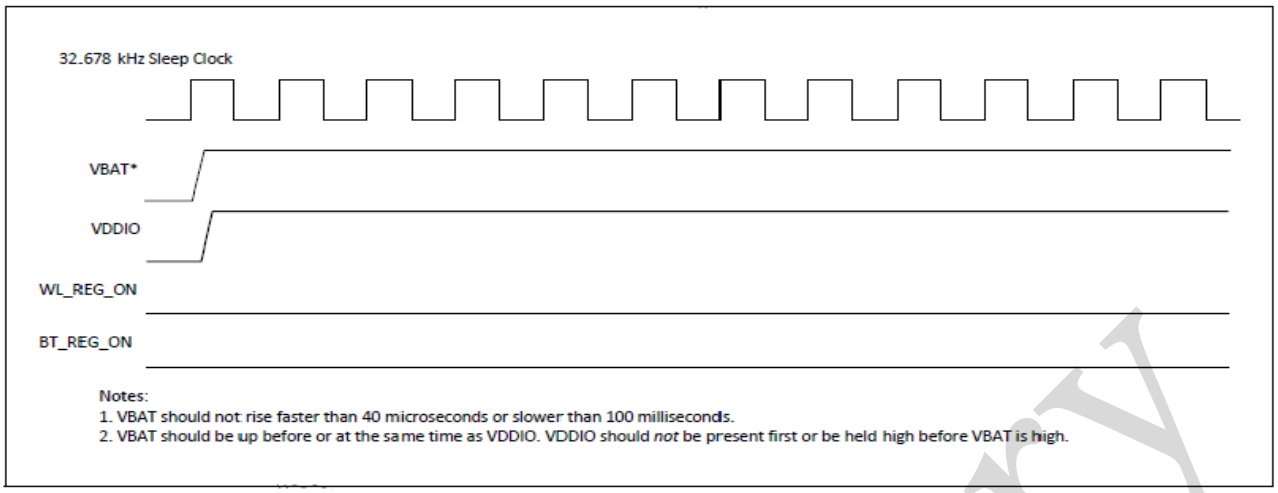
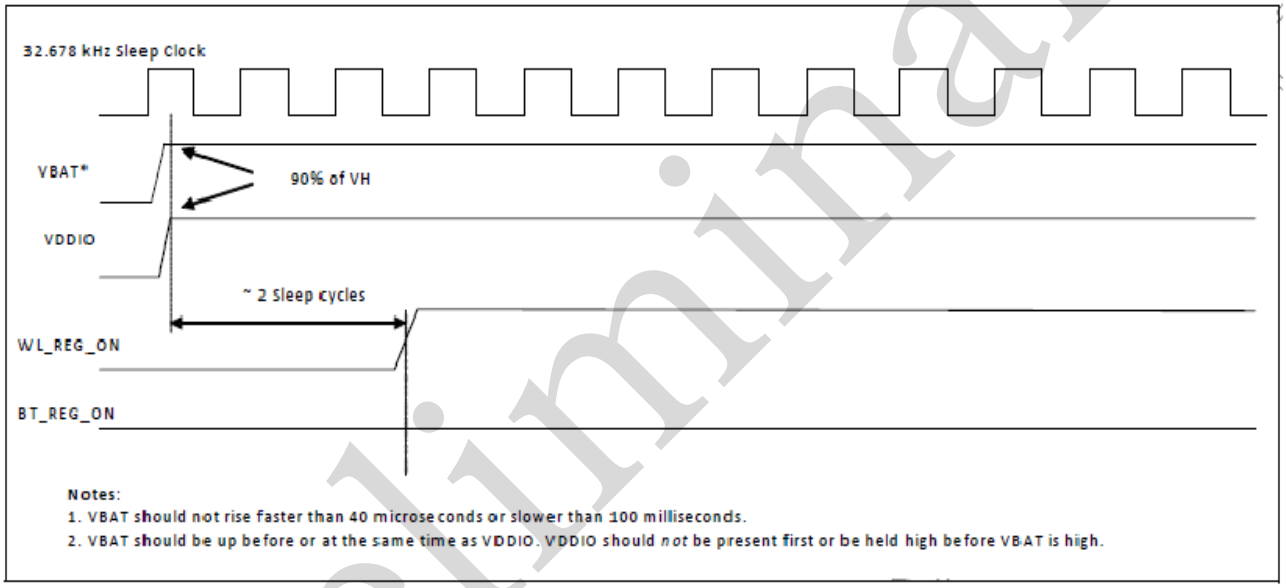
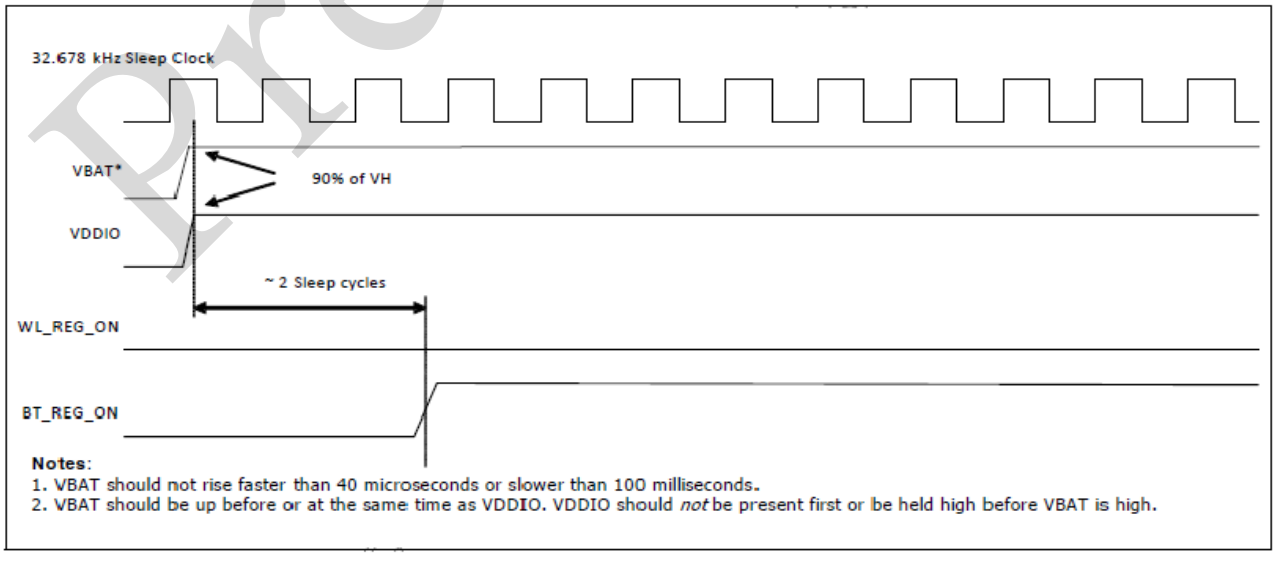


WLAN=OFF, Bluetooth=OFF



WLAN=ON, Bluetooth=OFF



WLAN=OFF, Bluetooth=ON

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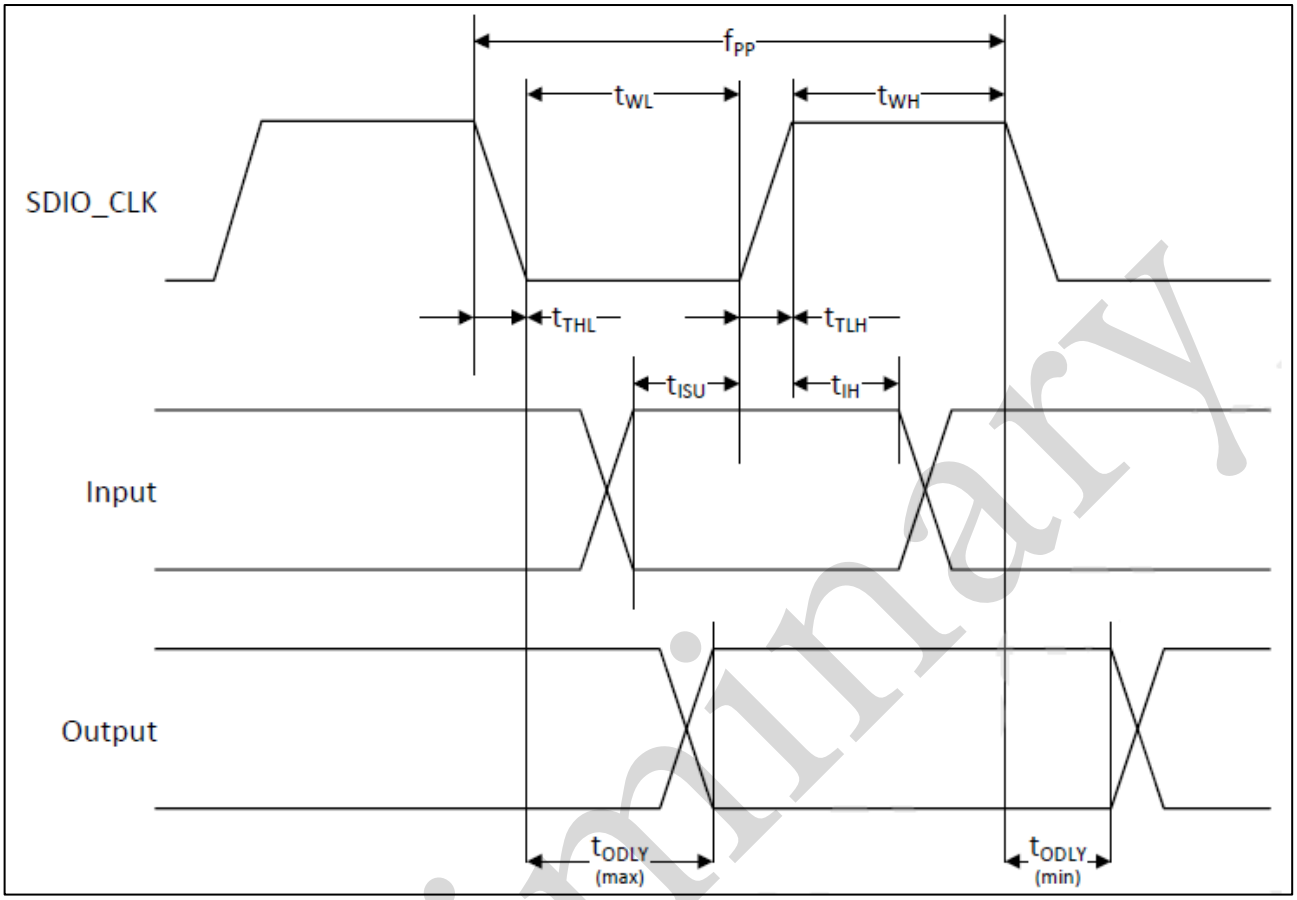
4.2 SDIO Default Mode Timing Diagram



Parameter	Symbol	Minimum	Typical	Maximum	Unit
SDIO CLK (ALL values are referred to minimum VIH and maximum VIL b)					
Frequency – Data Transfer mode	f_{PP}	0	-	25	MHz
Frequency – Identification mode	f_{OD}	0	-	400	kHz
Clock low time	t_{WL}	10	-	-	ns
Clock high time	t_{WH}	10	-	-	ns
Clock rise time	t_{TLH}	-	-	10	ns
Clock low time	t_{THL}	-	-	10	ns
Inputs：CMD, DAT(referenced to CLK)					
Input setup time	t_{ISU}	5	-	-	ns
Input hold time	t_{IH}	5	-	-	ns
Outputs：CMD, DAT(referenced to CLK)					
Output delay time, - Data Transfer mode	t_{ODLY}	0	-	14	ns
Output delay time, - Identification mode	t_{ODLY}	0	-	50	ns

a. Timing is based on CL ≤ 40 pF load on CMD and Data.

b. Min. (Vih) = 0.7 x VDDIO and max. (Vil) = 0.2 x VDDIO

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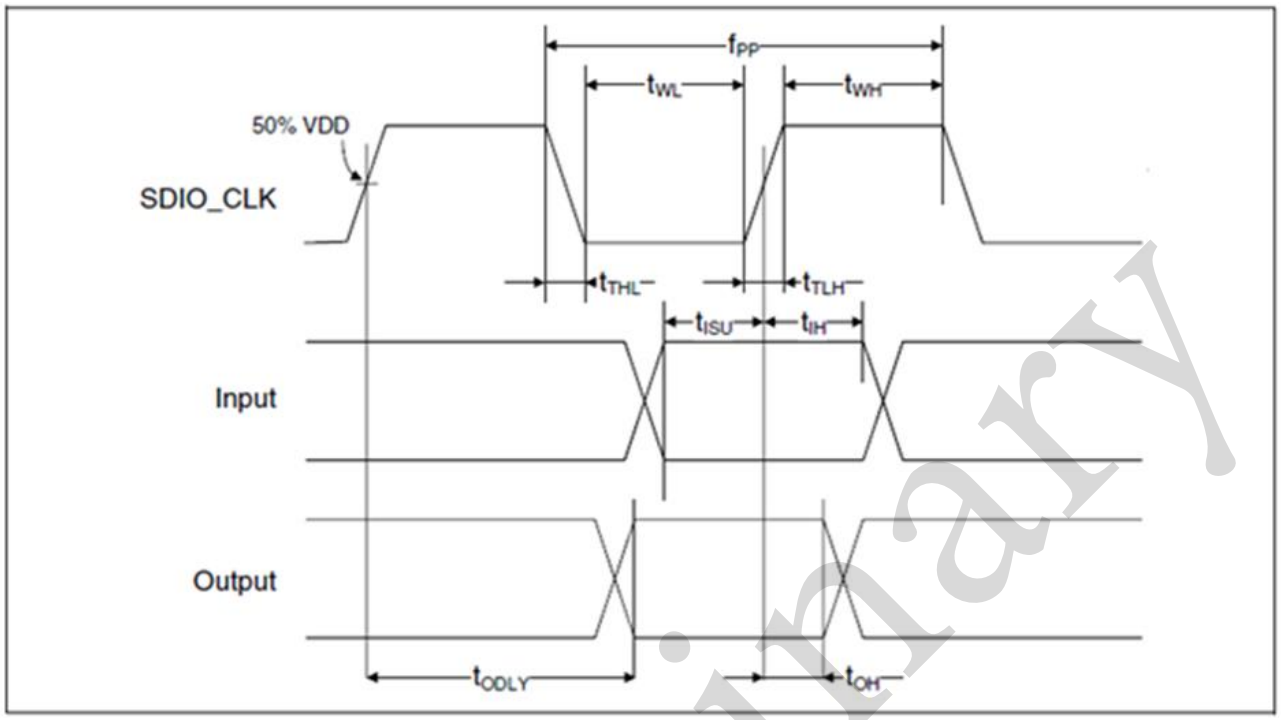
4.3 SDIO High Speed Mode Timing Diagram



Parameter	Symbol	Minimum	Typical	Maximum	Unit
SDIO CLK (ALL values are referred to minimum VIH and maximum VIL[b])					
Frequency – Data Transfer mode	f_{PP}	0	-	50	MHz
Frequency – Identification mode	f_{OD}	0	-	400	kHz
Clock low time	t_{WL}	7	-	-	ns
Clock high time	t_{WH}	7	-	-	ns
Clock rise time	t_{TLH}	-	-	3	ns
Clock low time	t_{THL}	-	-	3	ns
Inputs：CMD, DAT(referenced to CLK)					
Input setup time	t_{ISU}	6	-	-	ns
Input hold time	t_{IH}	2	-	-	ns
Outputs：CMD, DAT(referenced to CLK)					
Output delay time - Data Transfer mode	t_{ODLY}	-	-	14	ns
Output hold time	t_{OH}	2.5	-	-	ns
Total system capacitance(each line)	C_L			40	pF

a. Timing is based on CL ≤ 40 pF load on CMD and Data.

b. Min. (Vih) = 0.7 x VDDIO and max. (Vil) = 0.2 x VDDIO

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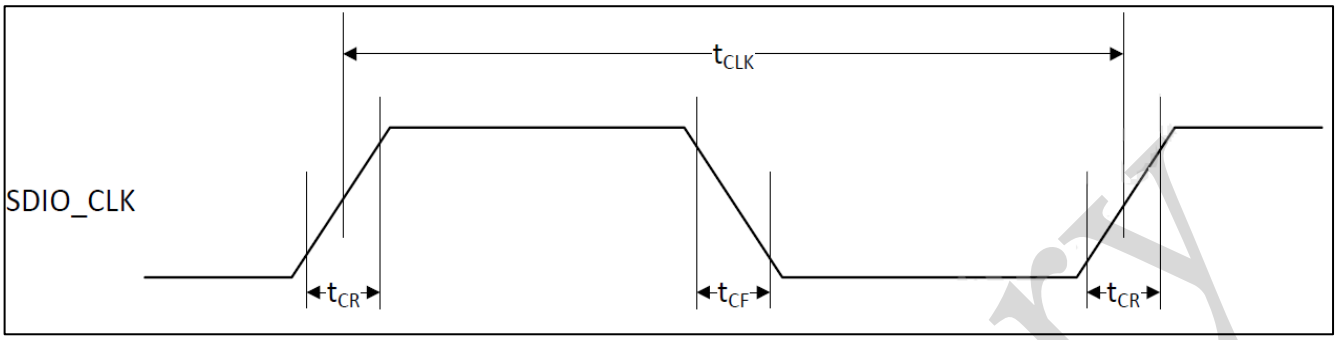
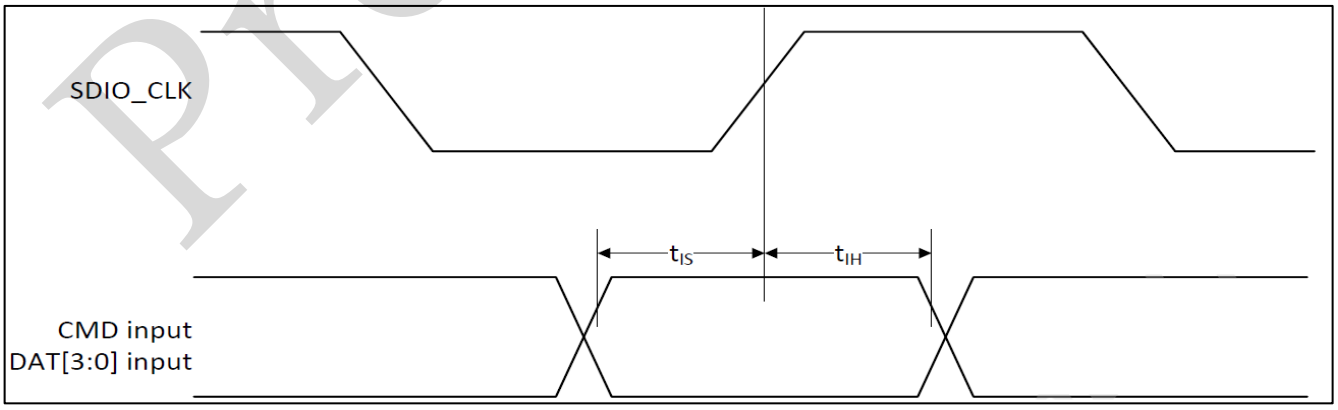
4.4 SDIO Bus Timing Specifications in SDR Modes

Clock timing (SDR Modes)



Parameter	Symbol	Minimum	Maximum	Unit	Comments
-	t_{CLK}	40	-	ns	SDR12 mode
		20	-	ns	SDR25mode
		10	-	ns	SDR50 mode
		4.8	-	ns	SDR104 mode
-	t_{CR},t_{CF}	-	0.2 x t_{CLK}	ns	t_{CR},t_{CF} < 2.00 ns (max) @100MHz, C_{CARD} = 10 pF t_{CR},t_{CF} < 0.96 ns (max) @208MHz, C_{CARD} = 10 pF
Clock duty	-	30	70	%	-

SDIO Bus Input timing (SDR Modes)



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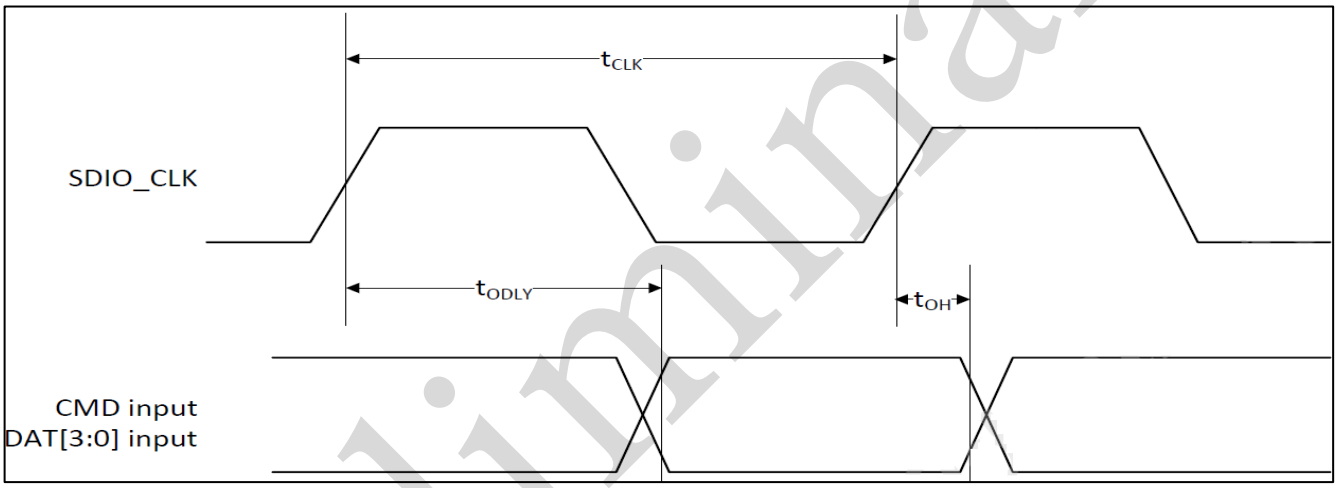
Symbol	Minimum	Maximum	Unit	Comments
SDR104 Mode				
t_{IS}	1.4	-	ns	C_{CARD} = 10 pF, VCT= 0.975V
t_{IH}	0.80	-	ns	C_{CARD} = 5 pF, VCT= 0.975V
SDR50 Mode				
t_{IS}	3.00	-	ns	C_{CARD} = 10 pF, VCT= 0.975V
t_{IH}	0.80	-	ns	C_{CARD} = 5 pF, VCT= 0.975V

SDIO Bus output timing (SDR Modes up to 100MHz)



Symbol	Minimum	Maximum	Unit	Comments
t_{ODLY}	-	7.5	ns	t_{CLK} ≥ 10 ns C_L = 30 pF using driver type B for SDR50
t_{ODLY}	-	14.0	ns	t_{CLK} ≥ 20 ns C_L = 40 pF using for SR12, SDR25
t_{OH}	1.5	-	ns	Hold time at the t_{ODLY} (min) C_L = 15 pF

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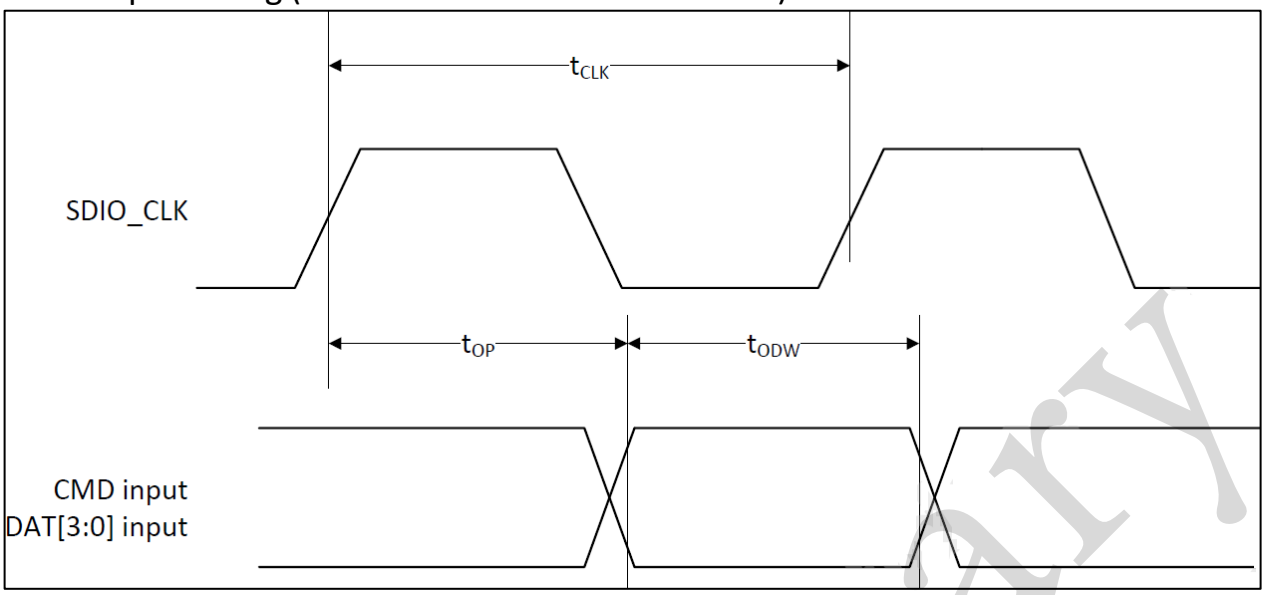
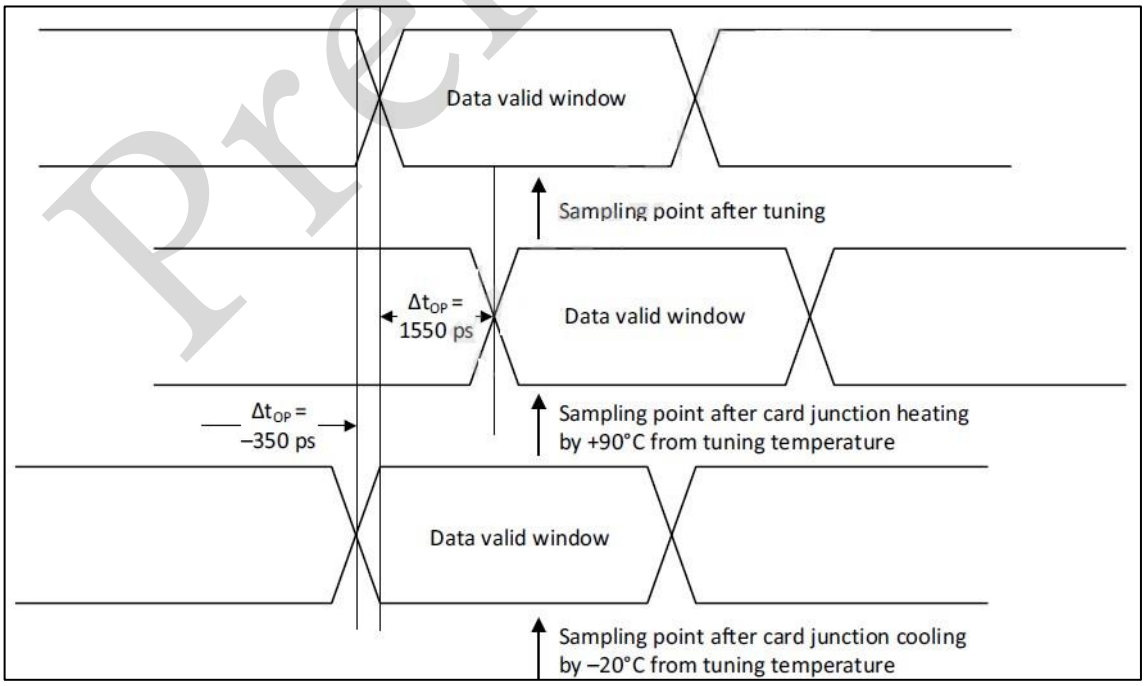
Card output timing (SDR Modes 100MHz to 208MHz)



Symbol	Minimum	Maximum	Unit	Comments
t_{OP}	0	2	UI	Card output phase
△t_{OP}	-350	+1550	ps	Delay variation due to temp. change after tuning
△t_{ODW}	0.60	-	UI	t_{ODW} = 2.88 ns @ 208MHz

- △t_{OP} = +1550 ps for junction temperature of △t_{OP} = 90 degrees during operation
- △t_{OP} = -350 ps for junction temperature of △t_{OP} = -20 degrees during operation
- △t_{OP} = +2600 ps for junction temperature of △t_{OP} = -20 to +125 degrees during operation

Δt_{OP} Consideration for Variable Data Window (SDR 104 Mode)



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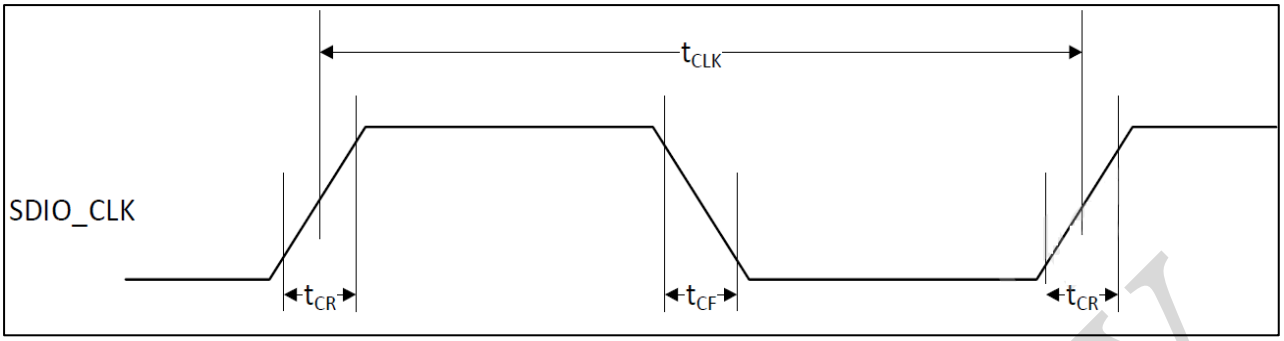
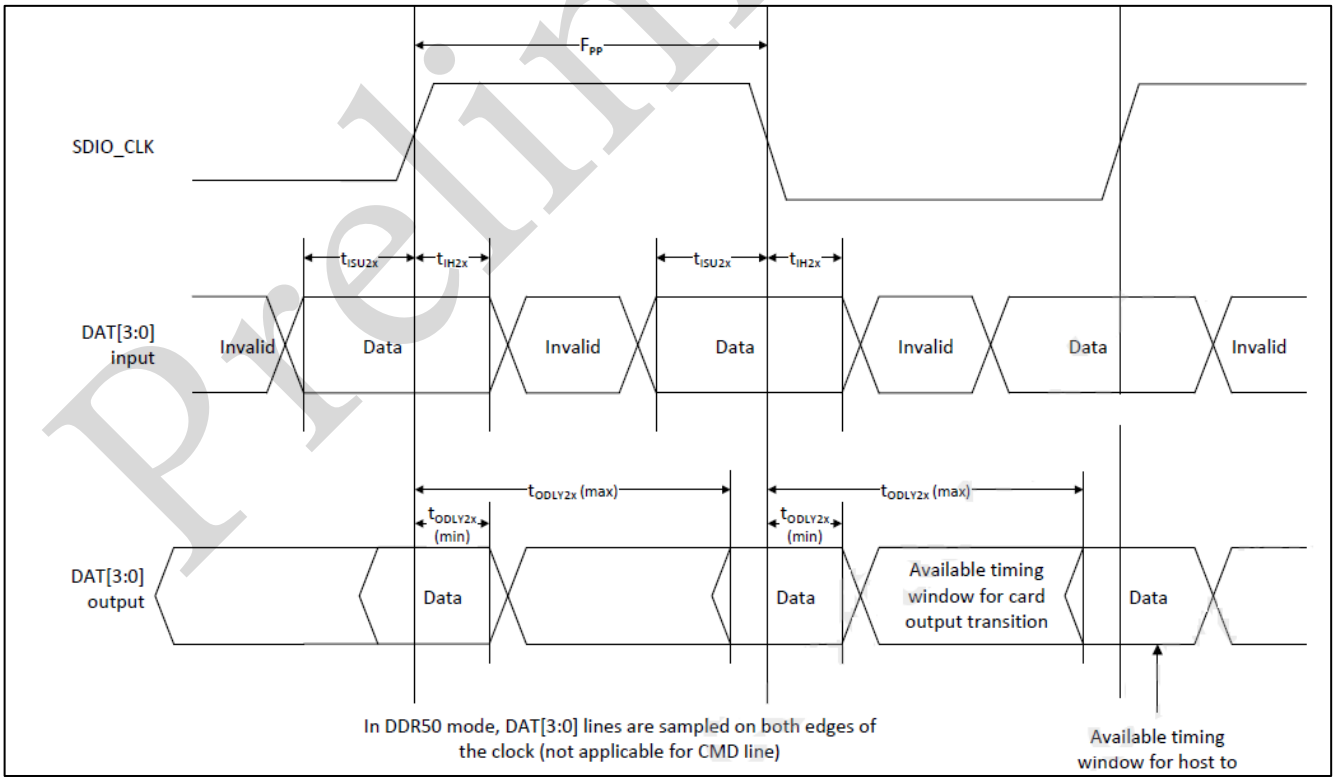
4.5 SDIO Bus Timing Specifications in DDR50 Mode



Parameter	Symbol	Minimum	Maximum	Unit	Comments
-	t_{CLK}	20	-	ns	DDR50 mode
-	t_{CR},t_{CF}	-	0.2 x t_{CLK}	ns	t_{CR},t_{CF} <4.00 ns(max) @ 50MHz C_{CARD}= 10 pF
Clock duty	-	45	55	%	-

Data Timing



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Parameter	Symbol	Minimum	Maximum	Unit	Comments
Input CMD					
Input setup time	t_{ISU}	6	-	ns	C_{CARD} < 10 pF (1 Card)
Input hold time	t_{IH}	0.8	-	ns	C_{CARD} < 10 pF (1 Card)
Output CMD					
Output delay time	t_{ODLY}	-	13.7	ns	C_{CARD} < 30 pF (1 Card)
Output hold time	t_{OH}	1.5	-	ns	C_{CARD} < 15 pF (1 Card)
Input DAT					
Input setup time	t_{ISU2x}	3	-	ns	C_{CARD} < 10 pF (1 Card)
Input hold time	t_{IH2x}	0.8	-	ns	C_{CARD} < 10 pF (1 Card)
Output DAT					
Output delay time	t_{ODLY2x}	-	7.5	ns	C_{CARD} < 25 pF (1 Card)
Output hold time	t_{ODLY2x}	1.5	-	ns	C_{CARD} < 15 pF (1 Card)

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4.6 PCIe Interface Description

The PCI Express(PCIe) core on the AP5881 is a high-performance serial I/O interconnect that is protocol compliant and electrically compatible with the PCI Express Base Specification v3.0 running at Gen1 speeds.

PCI Express Interface Parameters

Parameter	Symbol	Comments	Min.	Typ.	Max.	Unit
General[a]						
Baud rate	BPS	-	-	5	-	Gbaud
Reference clock peak -to-peak differential[b]	Vref	LVPECL, AC coupled	0.95	-	-	V
Receiver						
Differential termination	ZRX-DIFF-DC	Differential termination	80	100	120	Ω
DC impedance	ZRX-DC	DC common-mode impedance	40	50	60	Ω
Powered down termination (POS)	ZRX-HIGH-IMP-DC-POS	Powered down or RESET high impedance	100k	-	-	Ω
Powered down termination (NEG)	ZRX-HIGH-IMP-DC-NEG	Powered down or RESET high impedance	1k	-	-	Ω
Input voltage	VRX-DIFFp-p	AC coupled, differential p-p	175	-	-	mV
Jitter tolerance	TRX-EYE	Minimum receiver eye width	0.4	--	-	UI
Differential return loss	RLRX-DIFF	Differential return loss	10	-	-	dB
Common-mode return loss	RLRX-CM	Common-mode return loss	6	-	-	dB
Unexpected electrical idle enter detect threshold integration time	TRX-IDEL-DET-DIFF-ENTERTIME	An Unexpected electrical idle must be recognized no longer than this time to signal an unexpected idle condition	-	-	10	ms
Signal detect threshold	VRX-IDLE-DET-DIFFp-p	Electrical idle detect threshold	65	-	175	mV
Transmitter						
Output voltage	VTX-DIFFp-p	Differential p-p, programmable in 16 steps	0.8	-	1200	mV
Output voltage rise time	VTX-RISE	20% to 80%	0.125 (2.5 GT/s) 0.15 (5 GT/s)	-	-	UI
Output voltage fall time	VTX-FALL	80% to 20%	0.125 (2.5 GT/s) 0.15 (5 GT/s)	-	-	UI
RX detection voltage swing	VTX-RCV-DETECT	The amount of voltage change allowed during receiver detection	-	-	600	mV

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PCI Express Interface Parameters (Continued)

Parameter	Symbol	Comments	Min.	Typ.	Max.	Unit
TX AC peak common-mode voltage (5 GT/s)	VTX-CM-AC-PP	TX AC common-mode voltage (5 GT/s)	-	-	100	mV
TX AC peak common-mode voltage (2.5 GT/s)	VTX-CM-AC-P	TX AC common-mode voltage (2.5 GT/s)	-	-	20	mV
Absolute delta of DC common-mode voltage during L0 and electrical idle	VTX-CM-DC-ACTIVE-DLE-DELTA	Absolute delta of DC common-mode voltage during L0 and electrical idle	0	-	100	mV
Absolute delta of DC common-mode voltage between D+ and D-	VTX-CM-DC-LINE-DELTA	DC offset between D+ and D-	0	-	25	mV
Electrical idle differential peak output voltage	VTX-IDLE-DIFF-AC-p	Peak-to-peak voltage	0	-	20	mV
TX short circuit current	ITX-SHORT	Current limit when TX output is shorted to ground	-	-	90	mA
DC differential TX termination	ZTX-DIFF-DC	Low impedance defined during signaling (parameter is captured for 5.0 GHz by RLTX-DIFF)	80	-	120	Ω
Differential return loss	RLTX-DIFF	Differential return loss	10 (min) for 0.05: 1.25 GHz	-	-	dB
Common-mode return loss	RLTX-CM	Common-mode return loss	6	-	-	dB
TX eye width	TTX-EYE	Minimum TX eye width	0.75	-	-	UI

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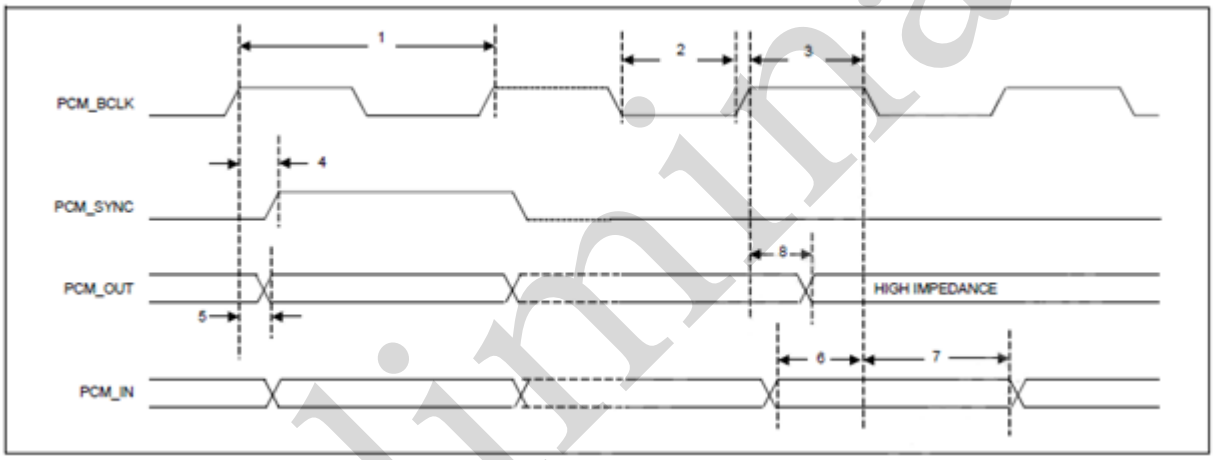
4.7 PCM Interface Description

The PCM Interface on the AP5881 can connect to linear PCM Codec devices in master or slave mode. In master mode, the AP5881 generates the PCM_CLK and PCM_SYNC signals, and in slave mode, these signals are provided by another master on the PCM interface and are inputs to the AP5881. The configuration of the PCM interface may be adjusted by the host through the use of vendor-specific HCI commands.

Short Frame Sync, Master Modem

PCM Timing Diagram (Short Frame Sync, Master Mode)



PCM Interface Timing Specifications (Short Frame Sync, Master Mode)

Reference	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency		-	12	MHz
2	PCM bit clock low	41	-	-	ns
3	PCM bit clock high	41	-	-	ns
4	PCM_SYNC delay	0	-	25	ns
5	PCM_OUT delay	0	-	25	ns
6	PCM_IN setup	8	-	-	ns
7	PCM_IN hold	8	-	-	ns
8	Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance	0	-	25	ns

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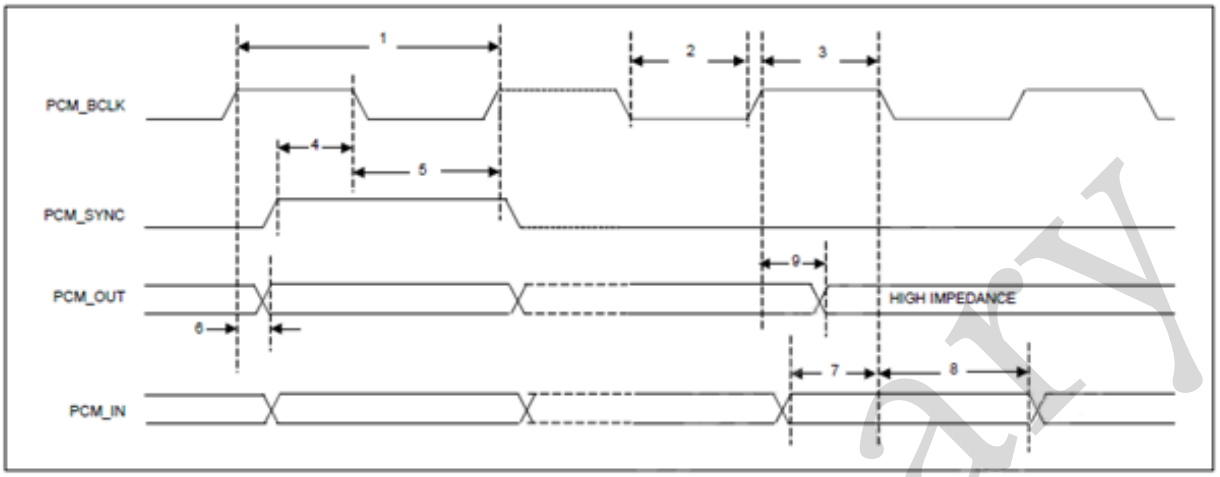
Short Frame Sync, Slave Mode

PCM Timing Diagram (Short Frame Sync, Slave Mode)



PCM Interface Timing Specifications (Short Frame Sync, Slave Mode)

Reference	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency		-	12	MHz
2	PCM bit clock low	41	-	-	ns
3	PCM bit clock high	41	-	-	ns
4	PCM_SYNC setup	8	-	-	ns
5	PCM_SYNC hold	8	-	-	ns
6	PCM_OUT delay	0	-	25	ns
7	PCM_IN setup	8	-	-	ns
8	PCM_IN hold	8	-	-	ns
9	Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance	0	-	25	ns

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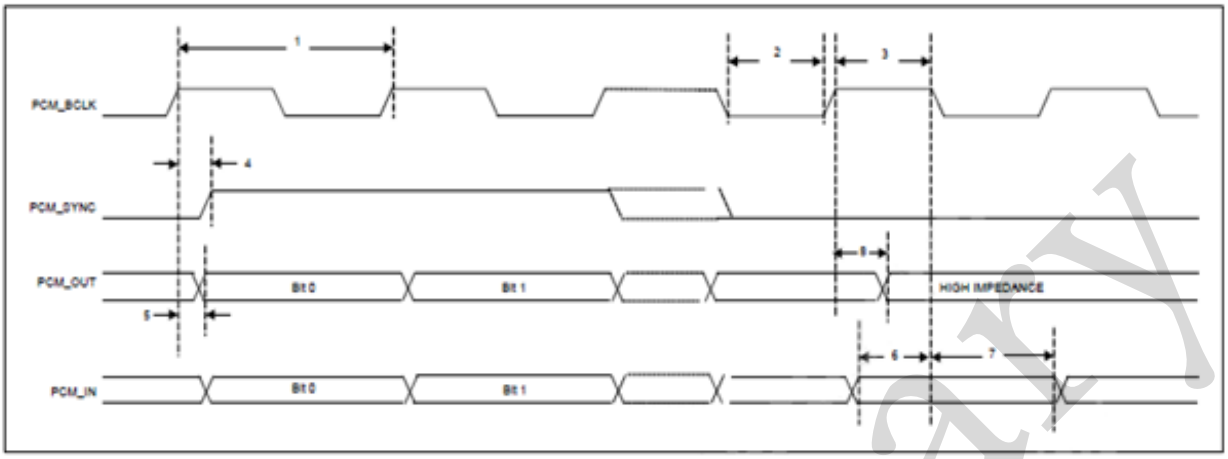
Long Frame Sync, Master Mode

PCM Timing Diagram (Long Frame Sync, Master Mode)



PCM Interface Timing Specifications (Long Frame Sync, Master Mode)

Reference	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency		-	12	MHz
2	PCM bit clock low	41	-	-	ns
3	PCM bit clock high	41	-	-	ns
4	PCM_SYNC delay	0	-	25	ns
5	PCM_OUT delay	0	-	25	ns
6	PCM_IN setup	8	-	-	ns
7	PCM_IN hold	8	-	-	ns
8	Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance	0	-	25	ns

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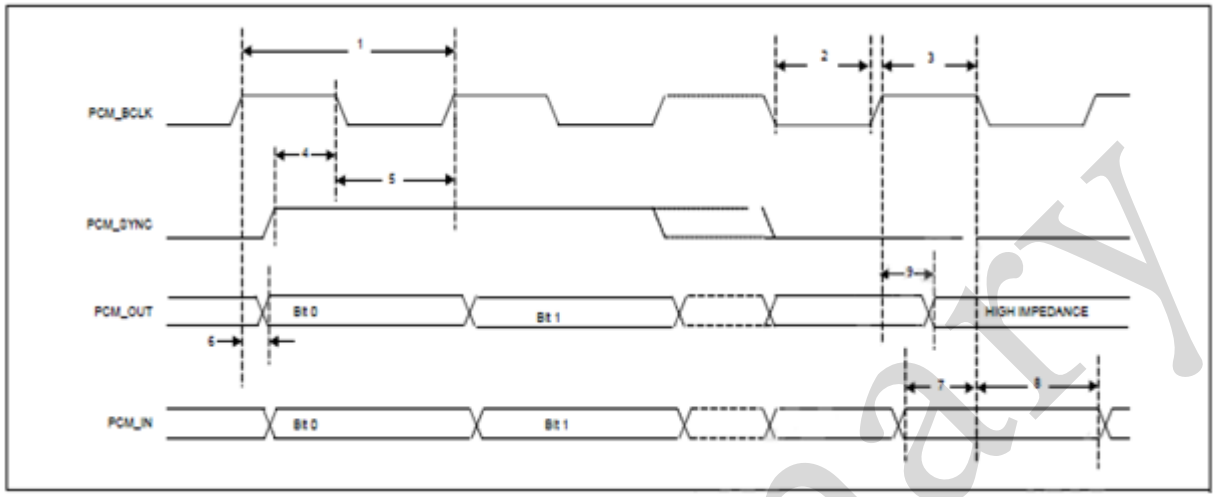
Long Frame Sync, Slave Mode

PCM Timing Diagram (Long Frame Sync, Slave Mode)



PCM Interface Timing Specifications (Long Frame Sync, Slave Mode)

Reference	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency		-	12	MHz
2	PCM bit clock low	41	-	-	ns
3	PCM bit clock high	41	-	-	ns
4	PCM_SYNC setup	8	-	-	ns
5	PCM_SYNC hold	8	-	-	ns
6	PCM_OUT delay	0	-	25	ns
7	PCM_IN setup	8	-	-	ns
8	PCM_IN hold	8	-	-	ns
9	Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance	0	-	25	ns

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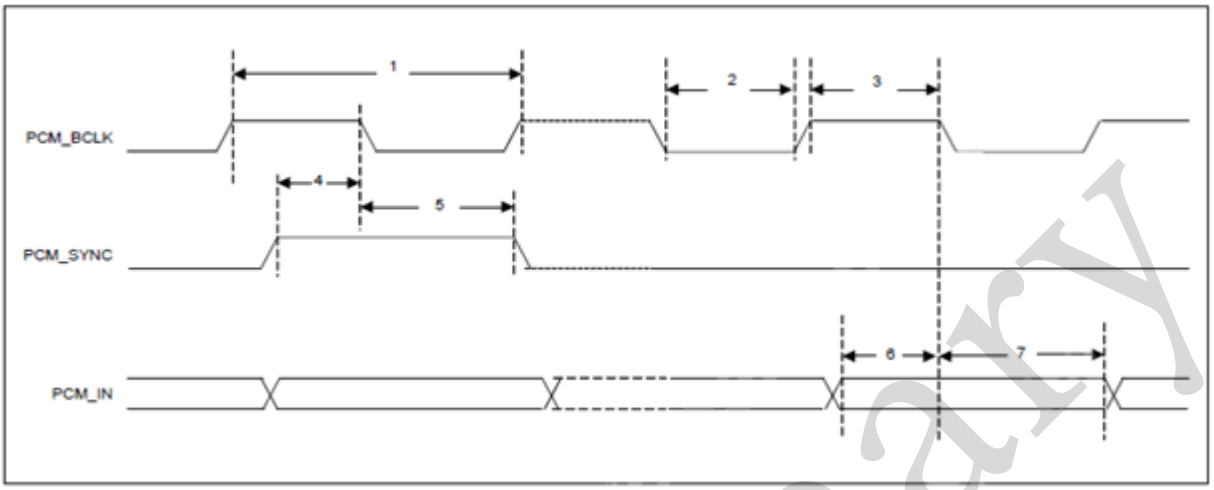
Short Frame Sync, Burst Mode

PCM Burst Mode Timing (Receive Only, Short Frame Sync)

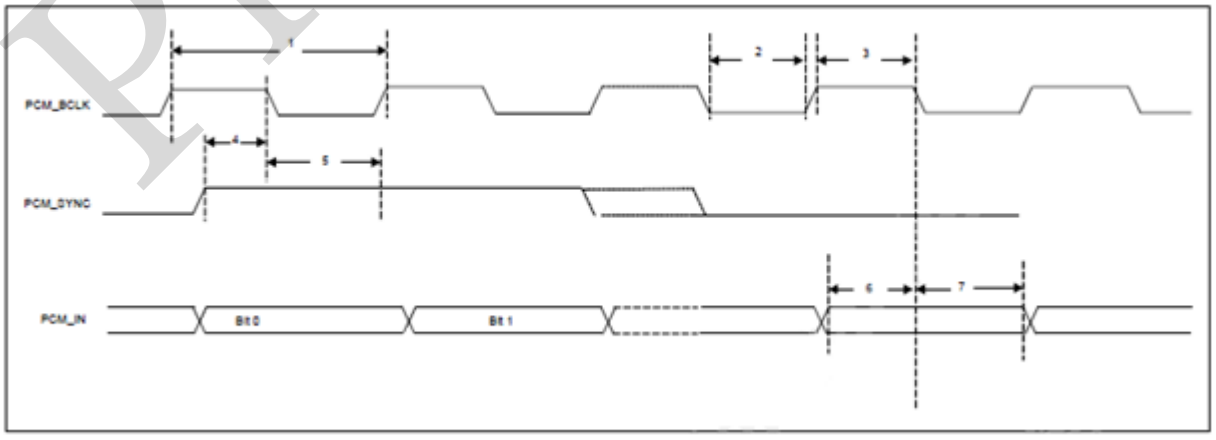


PCM Burst Mode (Receive Only, Short Frame Sync)

Reference	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency	-	-	24	MHz
2	PCM bit clock low	20.8	-	-	ns
3	PCM bit clock high	20.8	-	-	ns
4	PCM_SYNC setup	8	-	-	ns
5	PCM_SYNC hold	8	-	-	ns
6	PCM_IN setup	8	-	-	ns
7	PCM_IN hold	8	-	-	ns

Long Frame Sync, Burst Mode

PCM Burst Mode Timing (Receive Only, Long Frame Sync)



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PCM Burst Mode (Receive Only, Long Frame Sync)

Reference	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency	-	-	24	MHz
2	PCM bit clock low	20.8	-	-	ns
3	PCM bit clock high	20.8	-	-	ns
4	PCM_SYNC setup	8	-	-	ns
5	PCM_SYNC hold	8	-	-	ns
6	PCM_IN setup	8	-	-	ns
7	PCM_IN hold	8	-	-	ns

4.8 UART Interface Description

The UART is a standard 4-wire interface (RX, TX, RTS, and CTS) with adjustable baud rates from 9600 bps to 4.0 Mbps. The interface features an automatic baud rate detection capability that returns a baud rate selection. Alternatively, the baud rate may be selected through a vendor-specific UART HCI command.

UART has a 1040-byte receive FIFO and a 1040-byte transmit FIFO to support EDR. Access to the FIFOs is conducted through the AHB interface through either DMA or the CPU. The UART supports the Bluetooth 5.0 UART HCI specification: H4, a custom Extended H4, and H5. The default baud rate is 115.2 Kbaud.

The UART supports the 3-wire H5 UART transport, as described in the Bluetooth specification (Three-wire UART Transport Layer). Compared to H4, the H5 UART transport reduces the number of signal lines required by eliminating the CTS and RTS signals.

The UART can perform XON/XOFF flow control and includes hardware support for the Serial Line Input Protocol (SLIP). It can also perform wake-on activity. For example, activity on the RX or CTS inputs can wake the chip from a sleep state.

Normally, the UART baud rate is set by a configuration record downloaded after device reset, or by automatic baud rate detection, and the host does not need to adjust the baud rate. Support for changing the baud rate during normal HCI UART operation is included through a vendor-specific command that allows the host to adjust the contents of the baud rate registers. The UARTs operate correctly with the host UART as long as the combined baud rate error of the two devices is within ±2%.

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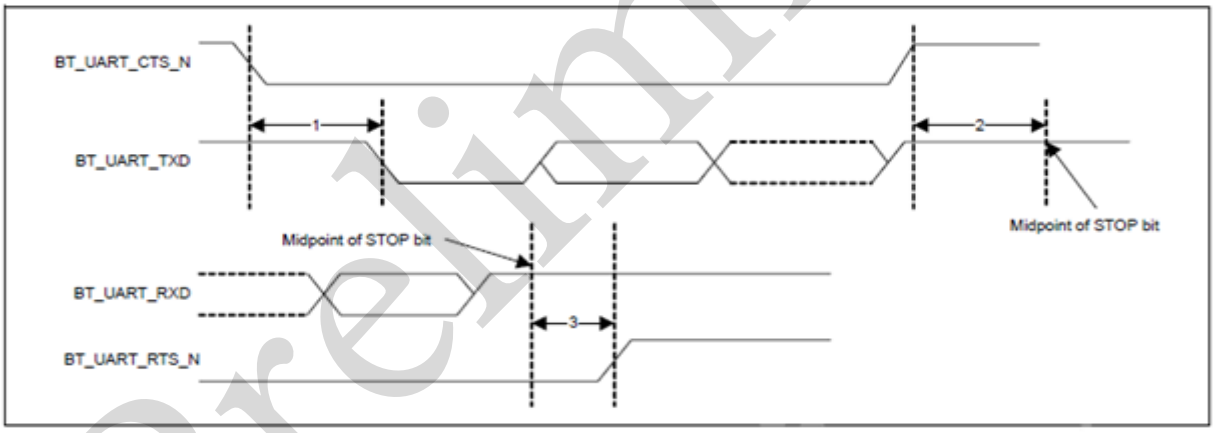
Example of Common Baud Rates

Desired Rate	Actual Rate	Error(%)
4000000	4000000	0.00
3692000	3692308	0.01
3000000	3000000	0.00
2000000	2000000	0.00
1500000	1500000	0.00
1444444	1454544	0.70
921600	923077	0.16
460800	461538	0.16
230400	230796	0.17
115200	115385	0.16
57600	57692	0.16
38400	38400	0.00
28800	28846	0.16
19200	19200	0.00
14400	14423	0.16
9600	9600	0.00

UART Timing



UART Timing Specifications

Ref	Characteristics	Min.	Typ.	Max.	Unit
1	Delay time, BT_UART_CTS_N low BT_UART_TXD valid	-	-	1.5	Bit periods
2	Setup time, BT_UART_CTS_N high before midpoint of stop bit	-	-	0.5	Bit periods
3	Delay time, midpoint of stop bit BT_UART_RTS_N high	-	-	0.5	Bit periods

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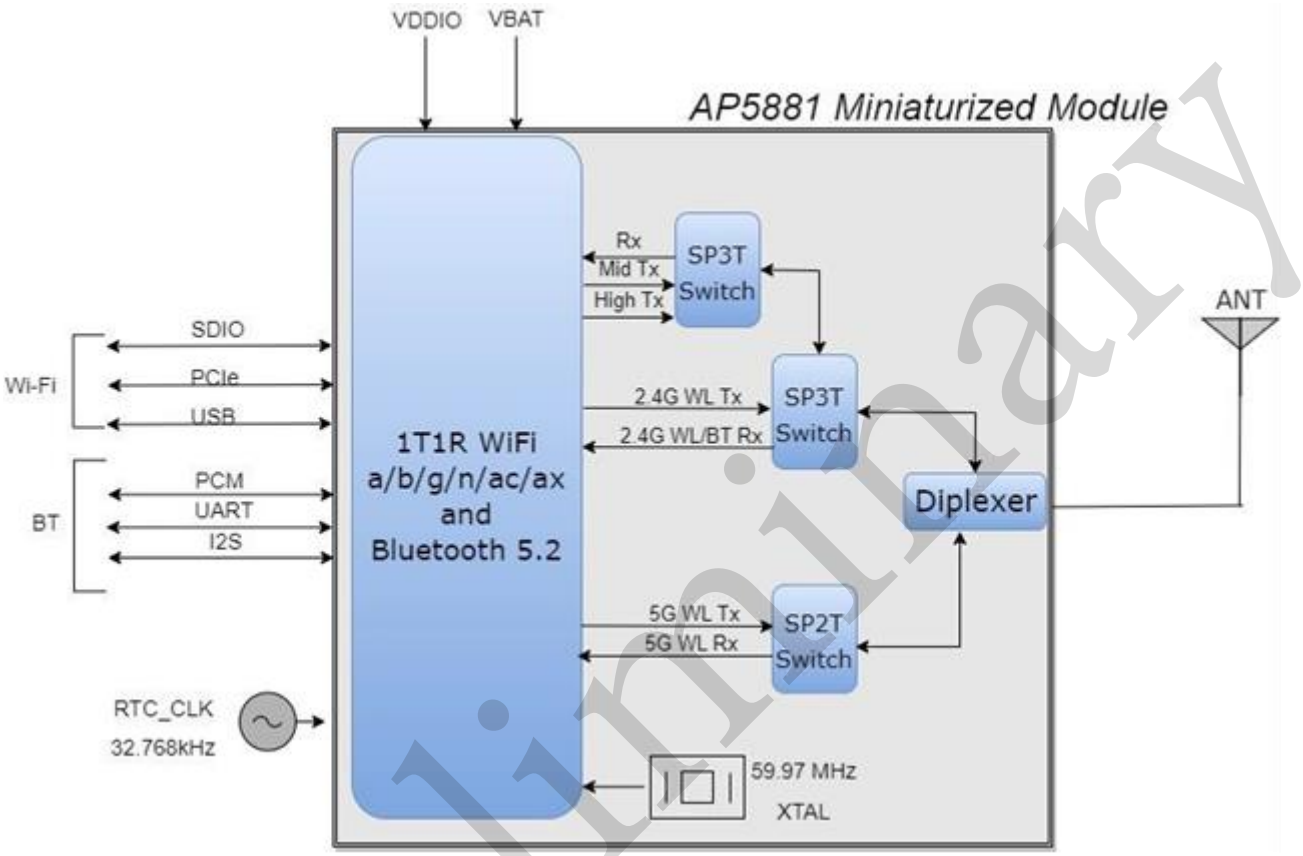
5. Block Diagram



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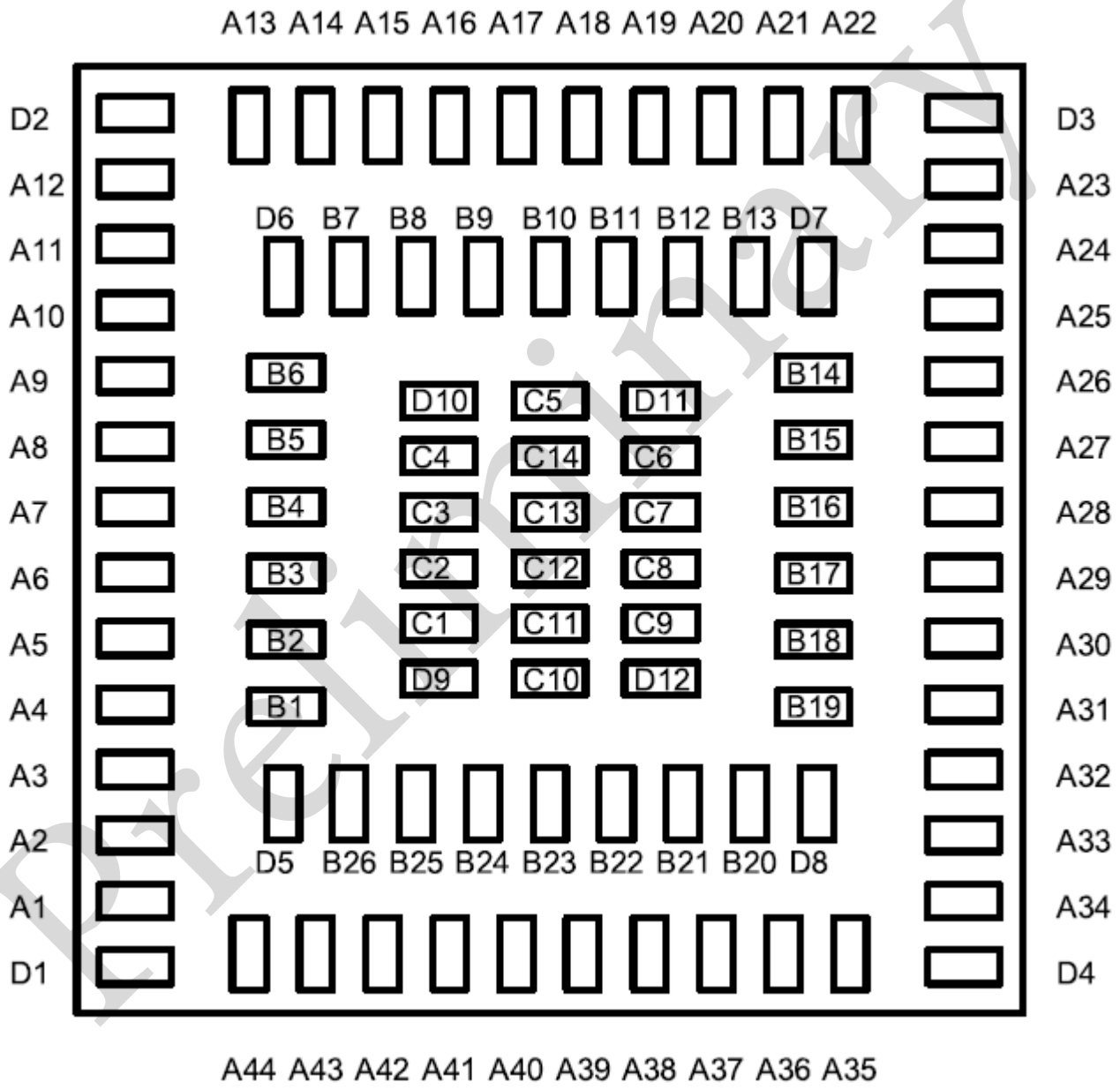
6. Pin Definition

6.1 Pin Outline

〈 **TOP VIEW** 〉



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6.2 Pin Table

NO	Name	Type	Description
RF Port			
A35	WL_ANT0	I/O	RF I/O port0
WLAN PCI Express Interface			
A21	PCIE_TX_P	O	PCI Express transmit data-Positive
A20	PCIE_TX_N	O	PCI Express transmit data-Negative
A16	PCIE_RX_N	I	PCI Express receive data-Negative
A17	PCIE_RX_P	I	PCI Express receive data-Positive
A19	PCIE_RCLK_P	I	PCI Express differential clock input-Positive
A18	PCIE_RCLK_N	I	PCI Express differential clock input-Negative
B21	PCIE_PME_L	OD	PCI power management event output
B20	PCIE_CLKREQ_L	OD	PCIe clock request
A2	PCIE_PREST_L	I	PCIe host indication to reset the device
WLAN SDIO Interface			
B11	SDIO_DATA_CMD	I/O	SDIO command line
B10	SDIO_DATA_3	I/O	SDIO data line 3
B9	SDIO_DATA_2	I/O	SDIO data line 2
B8	SDIO_DATA_1	I/O	SDIO data line 1
B7	SDIO_DATA_0	I/O	SDIO data line 0
B13	SDIO_DATA_CLK	I/O	SDIO clock line
Bluetooth UART Interface (level referred by VDDIO)			
C3	BT_UART_TXD	O	Bluetooth UART interface
C1	BT_UART_CTS_N	I	Bluetooth UART interface
C2	BT_UART_RTS_N	O	Bluetooth UART interface
C4	BT_UART_RXD	I	Bluetooth UART interface
Bluetooth PCM Interface (lever referred by VDDIO)			
B23	BT_PCM_OUT	O	BT PCM data output
B24	BT_PCM_SYNC	I/O	BT PCM sync ; can be master (output) or slave (input)
B25	BT_PCM_CLK	I/O	BT PCM CLK; can be master (output) or slave (input)
B26	BT_PCM_IN	I	BT PCM data input

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Reference Clock			
A7	LPO	I	External Low Power Clock input (32.768KHz)
A5	LHL_XTALI	I/O	32kHz XTAL input
A4	LHL_XTALO	I/O	32kHz XTAL output
GPIO and Control Signal (level referred by VDDIO)			
C12	WL_HOST_WAKE	O	WLAN to wake-up HOST and WL_GPIO_0
C11	WL_DEV_WAKE	I/O	This pin can be programmed by software to be a GPIO or a WLAN_DEV_WAKE output indicating that host wake-up should be performed.
C9	WL_GPIO_11	I/O	This pin can be programmed to be a GPIO, or the GCI external coexistence interface.
C8	WL_GPIO_10	I/O	This pin can be programmed to be a GPIO, or the GCI external coexistence interface.
C7	WL_GPIO_9	I/O	This pin can be programmed to be a GPIO, or the GCI external coexistence interface.
C6	WL_GPIO_8	I/O	This pin can be programmed to be a GPIO, or the GCI external coexistence interface.
B18	WL_GPIO_6	I/O	This pin can be programmed to be a GPIO, or the GCI external coexistence interface.
B17	WL_GPIO_5	I/O	This pin can be programmed to be a GPIO, or the GCI external coexistence interface.
D12	WL_GPIO_2	I/O	This pin can be programmed to be a GPIO, or the GCI external coexistence interface.
C14	GPIO_19	I/O	This pin can be programmed to be a GPIO, or the GCI external coexistence interface.
C13	GPIO_20	I/O	This pin can be programmed to be a GPIO, or the GCI external coexistence interface.
B1	BT_GPIO_2	I/O	Bluetooth general-purpose I/O
B2	BT_GPIO_3	I/O	Bluetooth general-purpose I/O
B3	BT_GPIO_4	I/O	Bluetooth general-purpose I/O
B4	BT_GPIO_5	I/O	Bluetooth general-purpose I/O
B5	BT_HOST_WAKE	O	Bluetooth device to wake-up HOST
B6	BT_DEV_WAKE	I	HOST wake-up Bluetooth device
B16	BT_REG_ON	I	Low asserting reset for Bluetooth core
B15	WL_REG_ON	I	Low asserting reset for WiFi core
A1	JTAG_SEL	I/O	JTAG, Just Floating.

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USB Interface			
A9	USB_5G	I	Input 5V voltage.
A11	USB_DM	I/O	USB Data -
A12	USB_DP	I/O	USB Data +
Power Supplies			
A39 **A40**	VBAT	P	Main power voltage source input
A42 **A43**	VDDIO	P	I/O Voltage supply input
A25	CSR_VLX	O	Internal Buck voltage generation pin
A23	CBUCK_0P72	I	Internal Buck voltage generation pin
A28 **A27**	ASR_VLX	O	Internal Analog Buck voltage generation pin
A31 **A30**	ABUCK_1P02	I	Internal Analog Buck voltage generation pin

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Ground			
A3	GND		Ground
A6			
A8			
A10			
A13~A15			
A22			
A24			
A26			
A29			
A32~A34			
A36~A38			
A41			
A44			
B12			
B14			
B19			
B22			
C5			
C10			
D1~D11			

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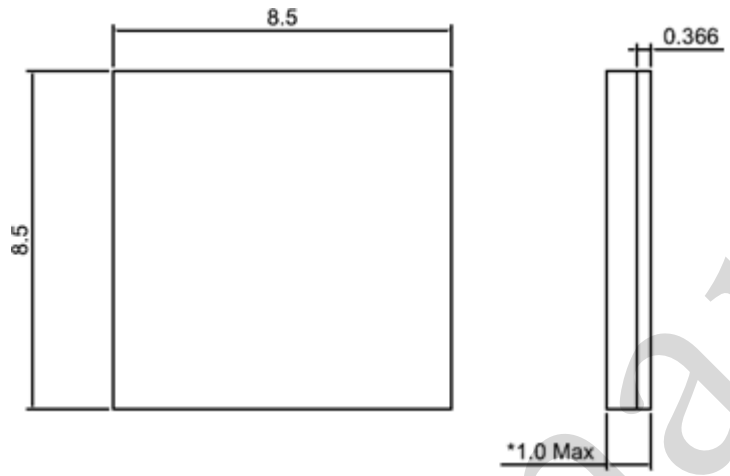
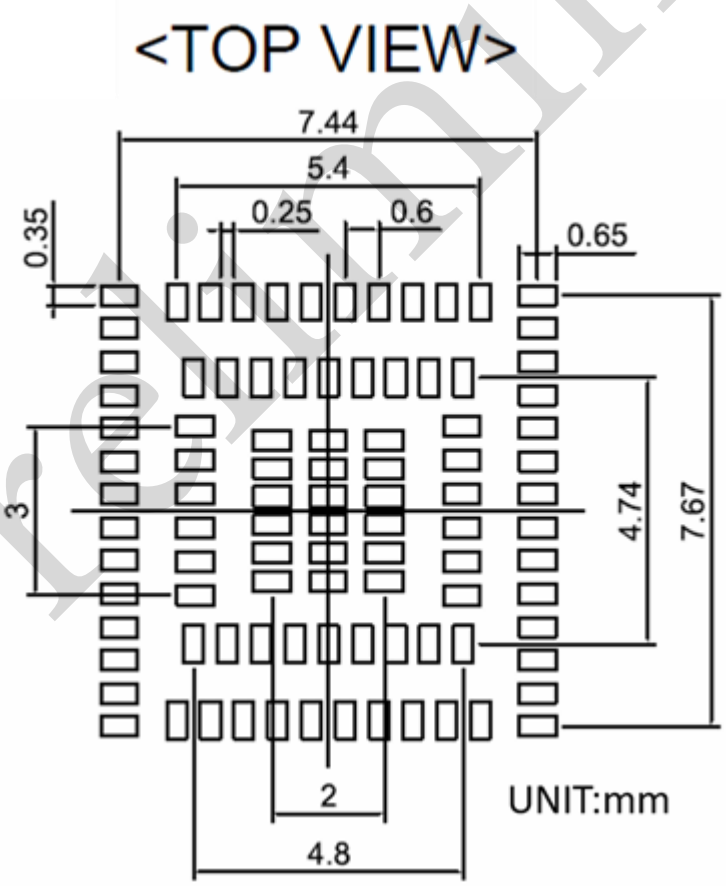
7. Mechanical Specifications

7.1 Module Dimensions





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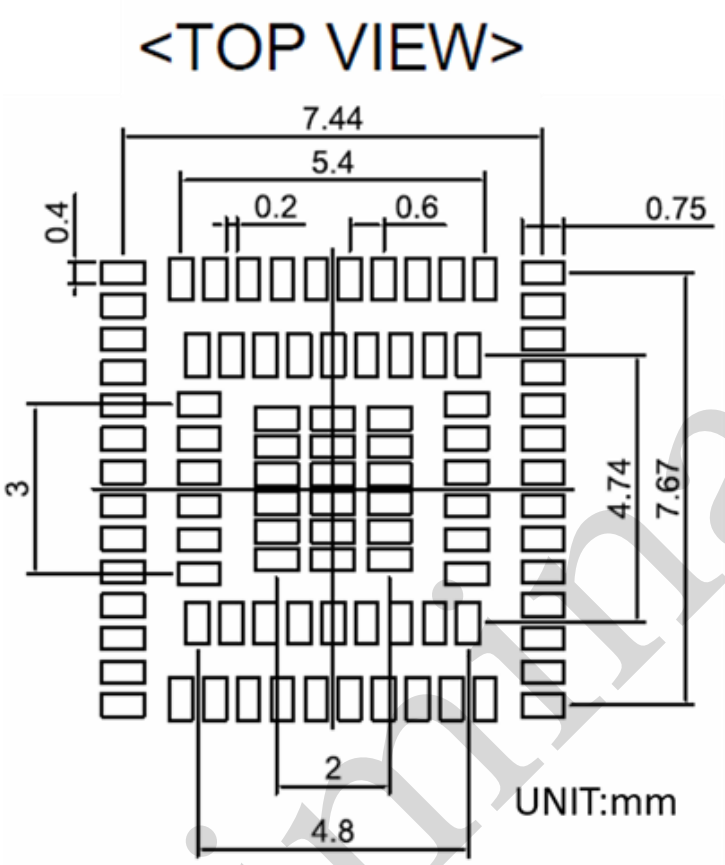
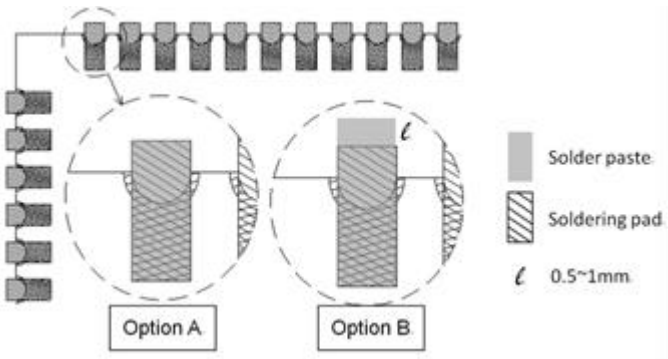
7.2 PCB Footprint



- Solder paste layer design is generally the same as recommended footprint

  If soldering quality with good wetting on upright side is essential for PQC, how to optimize the aperture design in the stencil to adjust the amount of solder paste would be crucial.

  In addition, a kind of stencil design with stepped thickness in partial area would be considered if the thickness of stencil is about 0.1mm or thinner. Please optimize the stencil design by manufacture engineer or contact SparkLAN FAE for assistance.



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8. External clock reference

External LPO signal characteristics

Parameter	Specification	Units
Nominal input frequency	32.768	kHz
Frequency accuracy	+/-25	ppm
Duty cycle	30 - 70	%
Input signal amplitude	1.8±0.09	V
Signal type	Square-wave or sine-wave	-
Input impedance	>100k <5	Ω pF
Clock jitter (integrated over 300Hz – 15KHz)	<1	Hz
Output high voltage	0.7Vio - Vio	V

External 37.4MHz X'TAL characteristics

Parameter	Specification	Units
Nominal input frequency – F0	59.97	MHz
Frequency Tolerance - Δ F / F 0 (At 25℃ +/- 3℃)	+/- 7	ppm
Operation Temperature Range - Topr	-30 ~ + 85	℃
Freq. Stability(over operating temperature) - TC Ref. to 25℃	+/- 10	ppm
Load capacitance - CL	8	pF
Equivalent Series Resistance – ESR	Max. 50	
Drive Level - DL	Typ. 50, Max. 100	uW
Insulation resistance – IR At 100Vdc	Min. 500	M

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8.1 SDIO Interface Description

The module supports SDIO version 3.0 for all 1.8V 4-bit UHSI speeds: SDR50 (100 Mbps), SDR104 (208MHz) and DDR50 (50MHz, dual rates), and backward compatible to SDIO version 2.0 default speed (25MHz) and high speed (50 MHz). It has the ability to stop the SDIO clock and map the interrupt signal into a GPIO pin. This 'out-of-band' interrupt signal notifies the host when the WLAN device wants to turn on the SDIO interface. The ability to force the control of the gated clocks from within the WLAN chip is also provided.

- Function 0 Standard SDIO function (Max BlockSize / ByteCount = 32B)
- Function 1 Backplane Function to access the internal System On Chip (SOC) address space (Max BlockSize / ByteCount = 64B)
- Function 2 WLAN Function for efficient WLAN packet transfer through DMA (Max BlockSize/ByteCount=512B)

SDIO Pin Description

SD 4-Bit Mode	
DATA0	Data Line 0
DATA1	Data Line 1 or Interrupt
DATA2	Data Line 2 or Read Wait
DATA3	Data Line 3
CLK	Clock
CMD	Command Line

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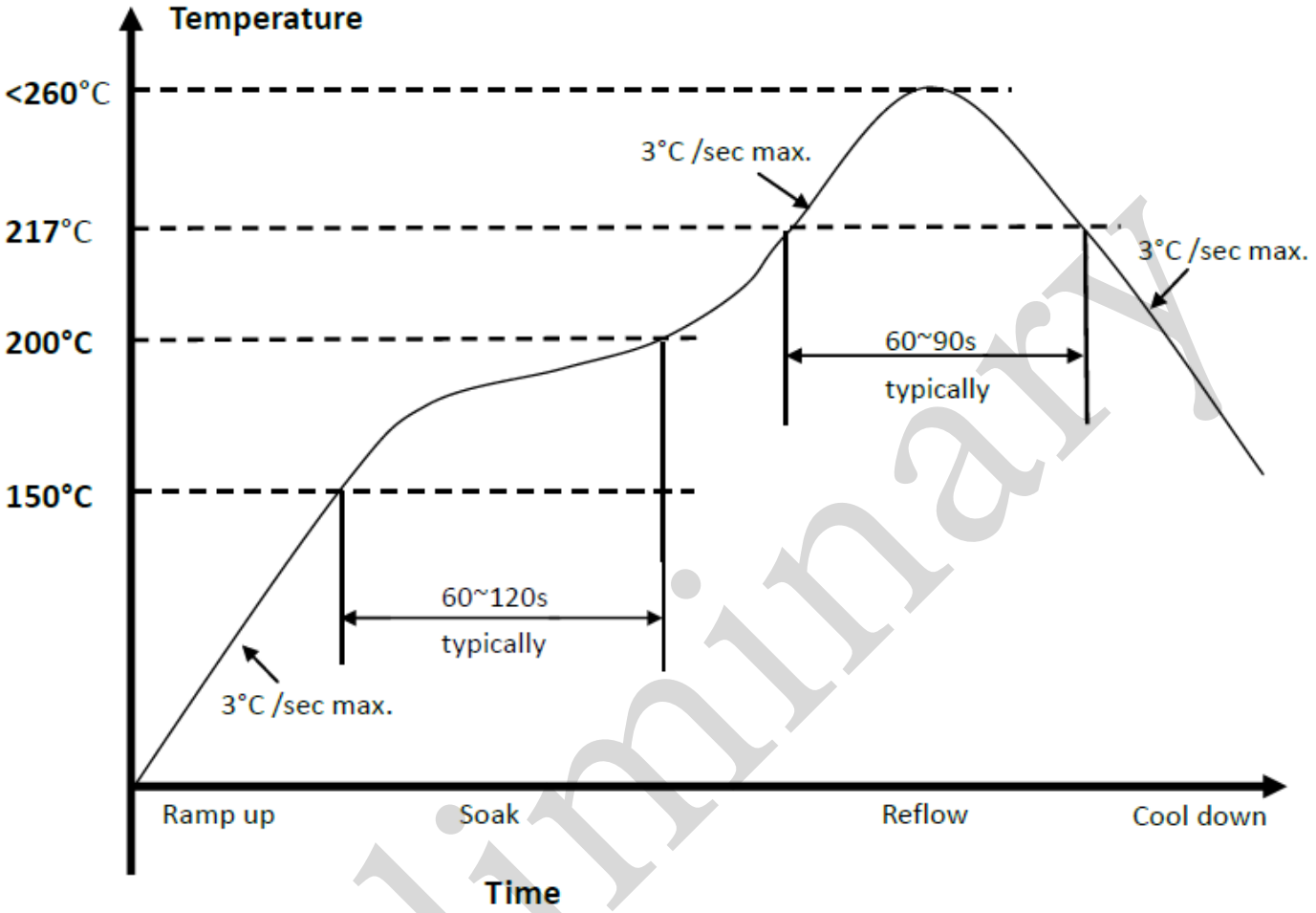
9. Recommended Reflow Profile



1. Referred to IPC/JEDEC standard
2. Peak Temperature: <260°C
3. Cycle of Reflow: 2 times max.
4. Adding Nitrogen (N2) to implement 2000ppm or less of oxygen concentration during reflow process is recommended.
5. If the shelf time is exceeded, be sure baking step to remove the moisture from the component

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9.1 Caution for SMT Preparation

Moisture Sensitivity Level: 4

1. Calculated shelf life in sealed bag: 12 months at <40℃ and <90% relative humidity (RH).
2. Peak package body temperature: 250℃.
3. After bag was opened, devices that will be subjected to reflow solder or other high temperature process must be
    a) Mounted within: 72 hours of factory conditions ≤30℃/60%RH or
    b) Stored per J-STD-033
4. Devices require bake before mounting, if:
    a) Humidity Indicator Card reads> 10% for level 2a - 5a devices or >60% for level 2 devices when read at 23±5℃
    b) 3a or 3b are not met.
5. If baking is required, refer to IPC/JEDEC J-STD-033 for bake procedure.

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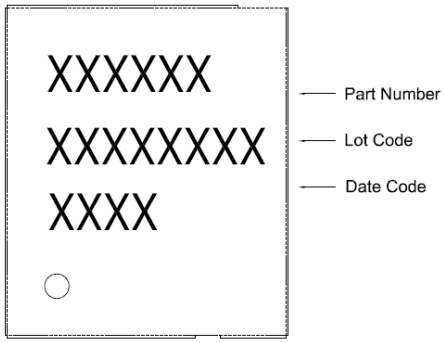
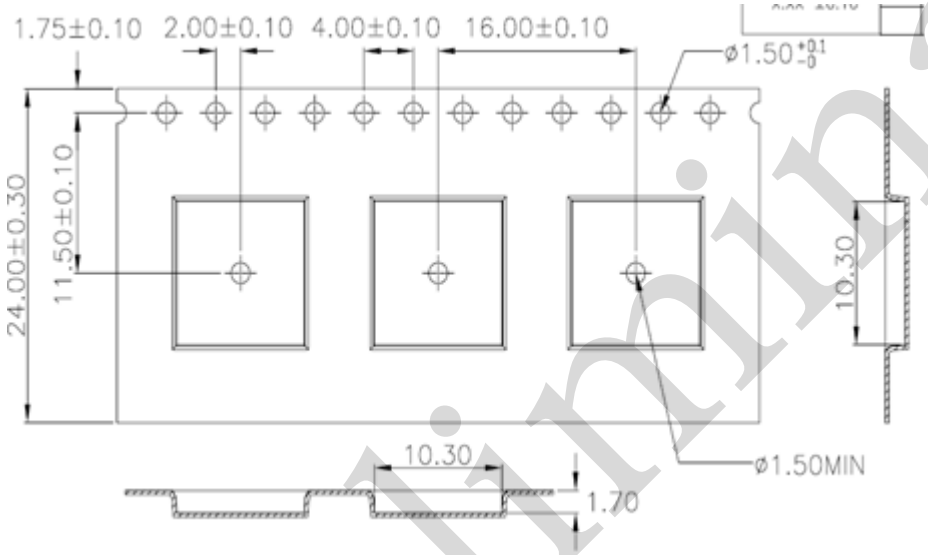
10. Package Information





1. 10 sprocket hole pitch cumulative tolerance ±0.20.
2. Carrier camber is within 1 mm in 250 mm.
3. Material: Black Conductive Polystyrene Alloy.
4. All dimensions meet EIA-481-D requirements.
5. Thickness: 0.30±0.05mm.
6. Component load per 13”reel: 1000 pcs

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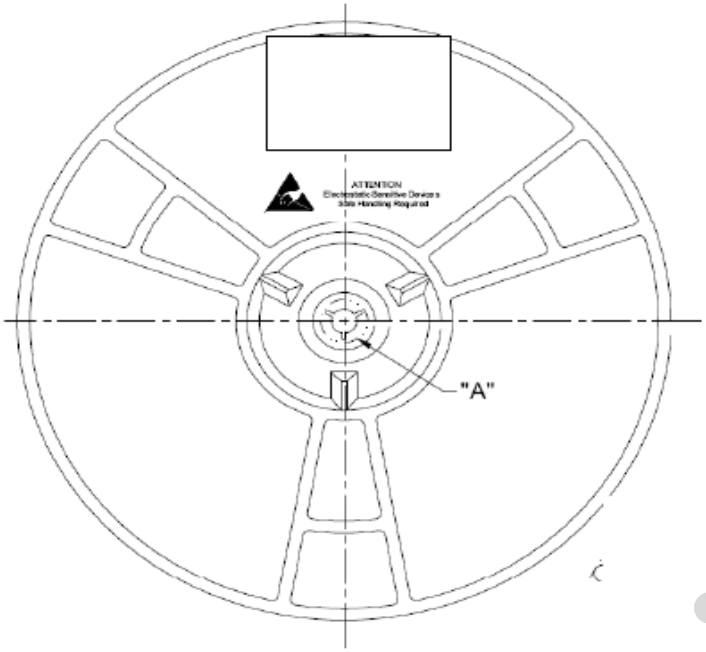

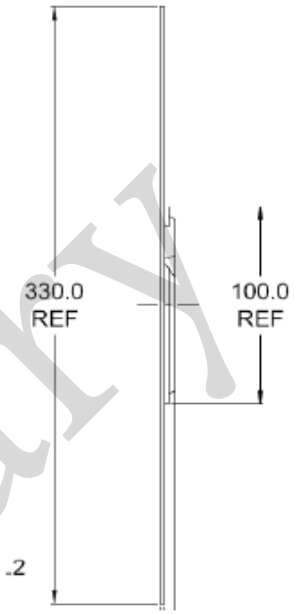

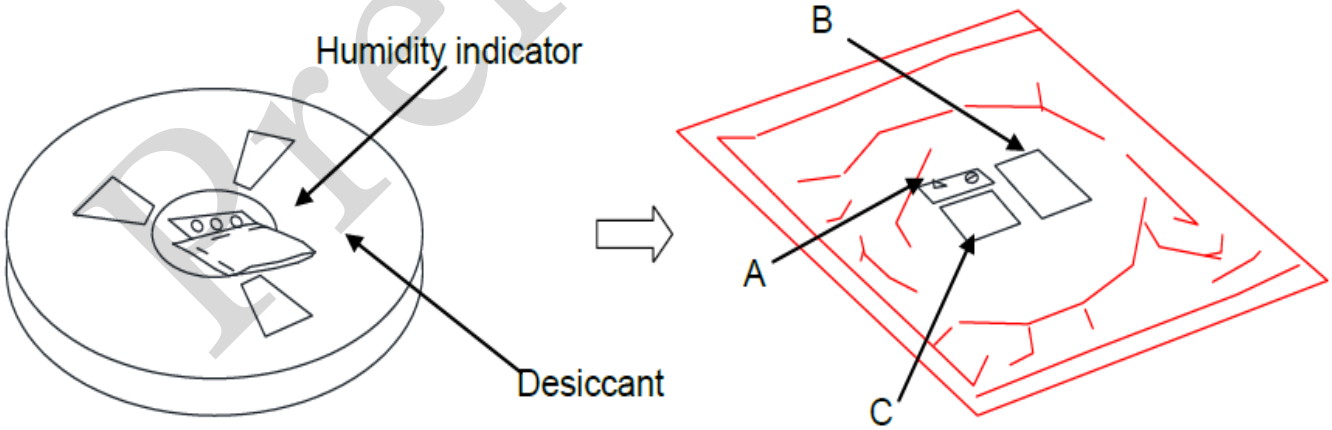

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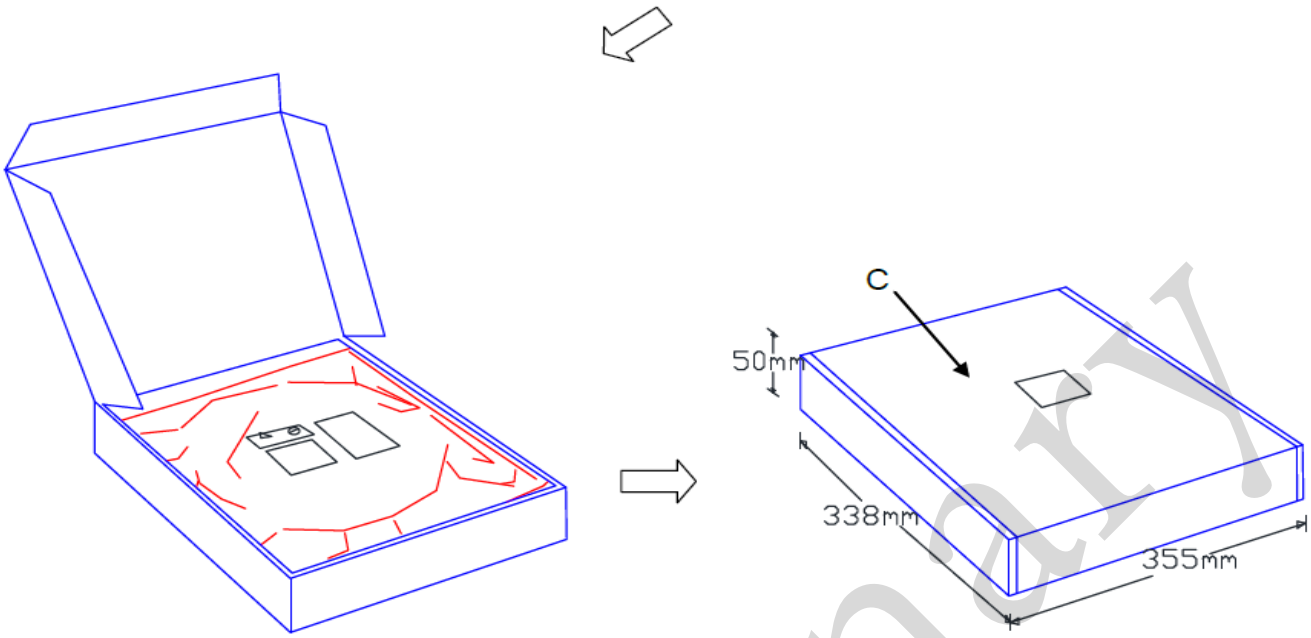

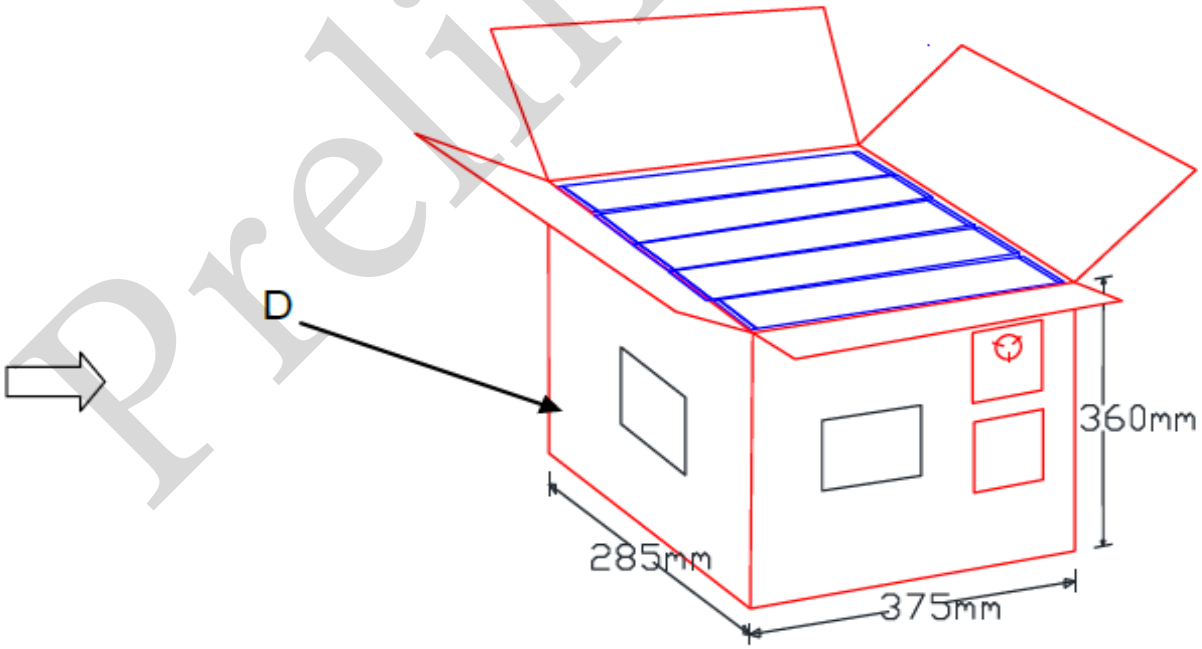

Note: 1 tape reel = 1 box = 1,000pcs
1 Carton = 5 box = 5,000pcs

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11. Ordering Information

Product Name	Part Number	Description
AP5881	TBD	11ax/ac/a/b/g/n 1T1R WiFi + BT5.2 Combo Sip Module

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