

Datasheet

AP6281

IEEE 802.11ax/ac/a/b/g/n 1x1

WiFi with Bluetooth5.2 Combo Sip Module

The revision history of the product specification

Version	Purpose	Date	Editor
1.0	Initial Doc	2022/1/7	Aaron

CONTENTS

1. Introduction	3
1.1 Product Overview	3
1.2 Product Features	3
1.2.1 WLAN	3
1.2.2 Bluetooth.....	3
2. Specification	4
2.1 General Specification	4
2.2 WiFi 2.4GHz RF Specification	5
2.3 WiFi 5GHz RF Specification	7
2.4 Bluetooth RF Specification	16
3. Electrical Characteristics	17
3.1 Absolute Maximum Ratings	17
3.2 Recommended Operating Rating	17
4. Host Interface Timing Diagram	18
4.1 Power-up Sequence Timing Diagram	18
4.2 SDIO Default Mode Timing Diagram	20
4.3 SDIO High Speed Mode Timing Diagram	21
4.4 SDIO Bus Timing Specifications in SDR Modes	22
4.5 SDIO Bus Timing Specifications in DDR50 Mode	25
4.6 PCM Interface Description	27
4.7 UART Interface Description	32
5. Block Diagram	34
6. Pin Definition	35
6.1 Pin Outline	35
6.2 Pin Table.....	35
7. Mechanical Specifications.....	38
7.1 Module Dimensions.....	38
7.2 PCB Footprint	39
8. External clock reference	40
8.1 SDIO Interface Description	41
9. Recommended Reflow Profile	42
9.1 Caution for SMT Preparation	43
10. Package Information.....	44
11. Ordering Information.....	47

1. Introduction

1.1 Product Overview

AP6281 is an 802.11ax (WiFi 6E) SiP Module, 802.11ax allow Increased capacity, faster speed, better coverage connections, improve the battery life of IoT sensors, and extend the range of Wi-Fi signals. By implementing the new 802.11ax standard with its unique features such as OFDMA, 1024QAM, Target Wake Time (TWT), and spatial reuse, the AP6281 module enables smooth streaming of high-resolution videos.

The fully Wi-Fi and Bluetooth functionalities module with seamless roaming capabilities and advance security, also it could interact with different vendors' 802.11a/b/g/n/ac/ax 1x1 Access Points with SISO standard and can accomplish up to speed of 600Mbps with single stream in 802.11ax to connect the wireless LAN. Furthermore AP6281 included USB 2.0 and SDIO v3.0 alternative interface for Wi-Fi, UART/ PCM interface for Bluetooth. In addition, this compact module is a total solution for a combination of Wi-Fi + BT technologies. The module is specifically developed for tablet, OTT box and portable devices.

1.2 Product Features

1.2.1 WLAN

- Lead Free design which is compliant with ROHS requirements.
- TX and RX low-density parity check (LDPC) support for improved range and power efficiency.
- Single-stream spatial multiplexing up to 600 Mbps data rate.
- 20, 40, 80 MHz channels with optional SGI (1024 QAM modulation).
- Supports standard SDIO v3.0 and USB2.0, compatible with SDIO v2.0 HOST interfaces.

1.2.2 Bluetooth

- BT host digital interface:
 - HCI UART (up to 4 Mbps)
 - PCM for audio data
- Complies with Bluetooth Core Specification Version 5.2 with provisions for supporting future specifications. With Bluetooth Class 1 or Class2 transmitter operation
- Supports extended synchronous connections (eSCO), for enhanced voice quality by allowing for retransmission of dropped packets

2. Specification

2.1 General Specification

Standards	IEEE 802.11 ax/ac/a/b/g/n 1T1R Wi-Fi + BT 5.2 Module Bluetooth V5.2, V5.0, V4.2, V4.1, V4.0 LE, V3.0+HS, V2.1+EDR
Chipset	Synaptics
Operating Frequency	2.400 GHz ~ 2.4835 GHz (2.4GHz ISM Band) 5.15~5.35GHz、5.47~5.725GHz、5.725~5.85GHz、5.955~6.415GHz 6.435~6.515GHz、6.535~6.855GHz、6.875~7.115GHz (5/6GHz UNII Band) Bluetooth: 2.402 GHz ~ 2.480 GHz
Modulation	WiFi: 802.11b: DSSS (DBPSK, DQPSK, CCK) 802.11g: OFDM (BPSK, QPSK, 16-QAM, 64-QAM) 802.11gn: OFDM (BPSK, QPSK, 16-QAM, 64-QAM) 802.11a: OFDM (BPSK, QPSK, 16-QAM, 64-QAM) 802.11an: OFDM (BPSK, QPSK, 16-QAM, 64-QAM) 802.11ac: OFDM (BPSK, QPSK, 16-QAM, 64-QAM, 256-QAM) 802.11ax: OFDMA (BPSK, QPSK, 16-QAM, 64-QAM, 256-QAM, 1024-QAM) BT: Header: GFSK Payload 2M: $\pi/4$ -DQPSK Payload 3M: 8-DPSK
Interface	WLAN: SDIO 3.0 / 2.0 and USB 2.0 Bluetooth: UART / PCM
Form Factor	SiP (System in Package) Stamp Type
Antenna	External
Dimension	L x W x H: 12mm(\pm 0.2mm) x 12mm(\pm 0.2mm) x 1.8mm(Max.)
Operating temperature	-30°C~85°C
Storage temperature	-40°C~125°C
Humidity (Non-Condensing)	10%~ 95% (Operating)
Weight	0.50g
Driver Support	Linux, Android

Note: The optimal RF performance specified in the data sheet, however, is guaranteed only -10 °C to +55 °C and 3.2V < VBAT < 3.8V without derating performance.

2.2 WiFi 2.4GHz RF Specification

Conditions: VBAT=3.3V; VDDIO=1.8V; Temp:25°C

Output Power, tolerance $\pm 1.5\text{dB}$						
The transmit EVM quality & spectrum mask are compliant with IEEE 802.11 standard						
802.11b	1Mbps	2Mbps	5.5Mbps	11Mbps		
	17	17	17	17		
802.11g	6、9Mbps	12、18Mbps	24Mbps	36Mbps	48Mbps	
	17	17	16	16	15	
	54Mbps					
	15					
802.11n 20MHz	MCS0~2	MCS3	MCS4	MCS5	MCS6	
	17	17	16	16	15	
	MCS7					
	15					
802.11ax 20MHz	HE0~2	HE3	HE4	HE5	HE6	
	17	17	16	16	15	
	HE7	HE8	HE9			
	15	14	13			
802.11ax_20MHz SISO	Data rate	Tones	Spec(dBm)	Data rate	Tones	Spec(dBm)
	HE0	26	17	HE6	26	15
		52	17		52	15
		106	17		106	15
		242	17		242	15
	HE1-2	26	17	HE7	26	15
		52	17		52	15
		106	17		106	15
		242	17		242	15
	HE3	26	17	HE8	26	14
		52	17		52	14
		106	17		106	14
		242	17		242	14
	HE4	26	16	HE9	26	13
		52	16		52	13
		106	16		106	13
		242	16		242	13
	HE5	26	16			
		52	16			
		106	16			
242		16				

Note: The specifications of RF output power are subject to change to fulfill the safety regulation and requirements in end-user product.

Sensitivity, tolerance ± 2 dB				
CCK modulation PER $\leq 8\%$ 、OFDM modulation PER $\leq 10\%$				
802.11b	Data Rate	Spec.(dBm)		
	1Mbps	-96		
	2Mbps	-90		
	5.5Mbps	-88		
	11Mbps	-87		
802.11g	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	6Mbps	-91	24Mbps	-83
	9Mbps	-88	36Mbps	-80
	12Mbps	-87	48Mbps	-76
	18Mbps	-85	54Mbps	-73
802.11n_20MHz	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	MCS0	-90	MCS4	-77
	MCS1	-85	MCS5	-75
	MCS2	-84	MCS6	-72
	MCS3	-80	MCS7	-71
802.11ax_20MHz	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	HE0	-90	HE6	-72
	HE1	-85	HE7	-71
	HE2	-84	HE8	-69
	HE3	-80	HE9	-68
	HE4	-77		
Maximum Input Level	802.11b: -10 dBm			
	802.11g/n/ax: -20 dBm			

2.3 WiFi 5GHz RF Specification

Conditions: VBAT=3.3V ; VDDIO=1.8V ; Temp:25°C

Output Power, tolerance ± 2 dB					
The transmit EVM quality & spectrum mask are compliant with IEEE 802.11 standard					
	Frequency (MHz)	6~9Mbps	12~18Mbps	24Mbps	36Mbps
	802.11a	5150~5845	16	16	16
5955~7115		15.5	15.5	15.5	15.5
Frequency (MHz)		48Mbps	54Mbps		
5150~5845		16	15		
5955~7115		15.5	14.5		
802.11n 20MHz	Frequency (MHz)	MCS0~2	MCS3	MCS4	MCS5
	5150~5845	16	16	16	16
	5955~7115	15.5	15.5	15.5	15.5
	Frequency (MHz)	MCS6	MCS7		
	5150~5845	15	14.5		
	5955~7115	14.5	14		
802.11n 40MHz	Frequency (MHz)	MCS0~2	MCS3	MCS4	MCS5
	5150~5845	15.5	15.5	15.5	15.5
	5955~7115	15	15	15	15
	Frequency (MHz)	MCS6	MCS7		
	5150~5845	15	14		
	5955~7115	14.5	13.5		
802.11ac 20MHz	Frequency (MHz)	MCS0~2	MCS3	MCS4	MCS5
	5150~5845	16	16	16	16
	5955~7115	15.5	15.5	15.5	15.5
	Frequency (MHz)	MCS6	MCS7	MCS8	
	5150~5845	15	14.5	12.5	
	5955~7115	14.5	14	12	

802.11ac 40MHz	Frequency (MHz)	MCS0~2	MCS3	MCS4	MCS5
	5150~5845	15.5	15.5	15.5	15.5
	5955~7115	15	15	15	15
	Frequency (MHz)	MCS6	MCS7	MCS8	MCS9
	5150~5845	15	14	12.5	11
	5955~7115	14.5	13.5	12	10.5
802.11ac 80MHz	Frequency (MHz)	MCS0~2	MCS3	MCS4	MCS5
	5150~5845	15.5	15.5	15.5	15.5
	5955~7115	15	15	15	15
	Frequency (MHz)	MCS6	MCS7	MCS8	MCS9
	5150~5845	15	14	12.5	11
	5955~7115	14.5	13.5	12	10.5
802.11ax 20MHz	Frequency (MHz)	MCS0~2	MCS3	MCS4	MCS5
	5150~5845	16	16	16	16
	5955~7115	15.5	15.5	15.5	15.5
	Frequency (MHz)	MCS6	MCS7	MCS8	MCS9
	5150~5845	15	14	12.5	11
	5955~7115	14.5	13.5	12	10.5
	Frequency (MHz)	MCS10	MCS11		
	5150~5845	10	10		
5955~7115	9.5	9.5			
802.11ax 40MHz	Frequency (MHz)	MCS0~2	MCS3	MCS4	MCS5
	5150~5845	15.5	15.5	15.5	15.5
	5955~7115	15	15	15	15
	Frequency (MHz)	MCS6	MCS7	MCS8	MCS9
	5150~5845	15	14	12.5	11
	5955~7115	14.5	13.5	12	10.5
	Frequency (MHz)	MCS10	MCS11		
	5150~5845	10	10		
5955~7115	9.5	9.5			

802.11ax 80MHz	Frequency (MHz)	MCS0~2	MCS3	MCS4	MCS5
	5150~5845	15.5	15.5	15.5	15.5
	5955~7115	15	15	15	15
	Frequency (MHz)	MCS6	MCS7	MCS8	MCS9
	5150~5845	15	14	12.5	11
	5955~7115	14.5	13.5	12	10.5
	Frequency (MHz)	MCS10	MCS11		
	5150~5845	9	9		
5955~7115	8.5	8.5			

Note: The specifications of RF output power are subject to change to fulfill the safety regulation and requirements in end-user product.

	Dara rate	Tones	Frequency	Spec.(dBm)
802.11ax_20MHz	HE0~2	26	5150~5845	16
			5955~7115	15.5
		52	5150~5845	16
			5955~7115	15.5
		106	5150~5845	16
			5955~7115	15.5
	242	5150~5845	16	
		5955~7115	15.5	
	HE3~4	26	5150~5845	16
			5955~7115	15.5
		52	5150~5845	16
			5955~7115	15.5
		106	5150~5845	16
			5955~7115	15.5
	242	5150~5845	16	
		5955~7115	15.5	
	HE5~7	26	5150~5845	14
			5955~7115	13.5
		52	5150~5845	14
			5955~7115	13.5
		106	5150~5845	14
			5955~7115	13.5
	242	5150~5845	14	
		5955~7115	13.5	

802.11ax_20MHz	HE8~9	26	5150~5845	11
			5955~7115	10.5
		52	5150~5845	11
			5955~7115	10.5
	106	5150~5845	11	
		5955~7115	10.5	
	242	5150~5845	11	
		5955~7115	10.5	
HE10~11	242	5150~5845	10	
		5955~7115	9.5	
802.11ax_40MHz	Dara rate	Tones	Frequency	Spec.(dBm)
	HE0~2	26	5150~5845	15.5
			5955~7115	15
		52	5150~5845	15.5
			5955~7115	15
		106	5150~5845	15.5
			5955~7115	15
		242	5150~5845	15.5
			5955~7115	15
	HE3~4	26	5150~5845	15.5
			5955~7115	15
		52	5150~5845	15.5
			5955~7115	15
		106	5150~5845	15.5
			5955~7115	16
		242	5150~5845	15.5
			5955~7115	15
	484	5150~5845	15.5	
		5955~7115	15	

	Dara rate	Tones	Frequency	Spec.(dBm)
802.11ax_40MHz	HE5~7	26	5150~5845	14
			5955~7115	13.5
		52	5150~5845	14
			5955~7115	13.5
		106	5150~5845	14
			5955~7115	13.5
	242	5150~5845	14	
		5955~7115	13.5	
	484	5150~5845	14	
		5955~7115	13.5	
	HE8~9	26	5150~5845	11
			5955~7115	10.5
		52	5150~5845	11
			5955~7115	10.5
		106	5150~5845	11
			5955~7115	10.5
	242	5150~5845	11	
		5955~7115	10.5	
	484	5150~5845	11	
		5955~7115	10.5	
HE10~11	242	5150~5845	10	
		5955~7115	9.5	
	484	5150~5845	19	
		5955~7115	9.5	

	Dara rate	Tones	Frequency	Spec.(dBm)
802.11ax_80MHz	HE0~2	26	5150~5845	15.5
			5955~7115	15
		52	5150~5845	15.5
			5955~7115	15
		106	5150~5845	15.5
			5955~7115	15
		242	5150~5845	15.5
			5955~7115	15
		484	5150~5845	15.5
			5955~7115	15
		996	5150~5845	15.5
			5955~7115	15
	HE1~2	26	5150~5845	15.5
			5955~7115	15
		52	5150~5845	15.5
			5955~7115	15
		106	5150~5845	15.5
			5955~7115	15
		242	5150~5845	15.5
			5955~7115	15
		484	5150~5845	15.5
			5955~7115	15
		996	5150~5845	15.5
			5955~7115	15
HE3~4	26	5150~5845	15.5	
		5955~7115	15	
	52	5150~5845	15.5	
		5955~7115	15	
	106	5150~5845	15.5	
		5955~7115	15	
	242	5150~5845	15.5	
		5955~7115	15	
	484	5150~5845	15.5	
		5955~7115	15	
	996	5150~5845	15.5	
		5955~7115	15	

	Dara rate	Tones	Frequency	Spec.(dBm)
802.11ax_80MHz	HE5~7	26	5150~5845	14
			5955~7115	13.5
		52	5150~5845	14
			5955~7115	13.5
		106	5150~5845	14
			5955~7115	13.5
		242	5150~5845	14
			5955~7115	13.5
		484	5150~5845	14
			5955~7115	13.5
		996	5150~5845	14
			5955~7115	13.5
	HE8~9	26	5150~5845	11
			5955~7115	10.5
		52	5150~5845	11
			5955~7115	10.5
		106	5150~5845	11
			5955~7115	10.5
		242	5150~5845	11
			5955~7115	10.5
		484	5150~5845	11
			5955~7115	10.5
		996	5150~5845	11
			5955~7115	10.5
HE10~11	242	5150~5845	9	
		5955~7115	8.5	
	484	5150~5845	9	
		5955~7115	8.5	
	996	5150~5845	9	
		5955~7115	8.5	

Sensitivity, tolerance ± 1.5 dB				
CCK modulation PER $\leq 8\%$ 、 OFDM modulation PER $\leq 10\%$				
	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
802.11a	6Mbps	-90	24Mbps	-83
	9Mbps	-90	36Mbps	-80
	12Mbps	-88	48Mbps	-75
	18Mbps	-86	54Mbps	-73
802.11n_20MHz	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	6Mbps	-90	24Mbps	-79
	9Mbps	-88	36Mbps	-76
	12Mbps	-86	48Mbps	-73
	18Mbps	-83	54Mbps	-72
802.11n_40MHz	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	MCS0	-88	MCS4	-77
	MCS1	-86	MCS5	-72
	MCS2	-83	MCS6	-70
	MCS3	-80	MCS7	-69
802.11ac_20MHz	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	MCS0	-90	MCS5	-75
	MCS1	-88	MCS6	-73
	MCS2	-86	MCS7	-70
	MCS3	-83	MCS8	-68
	MCS4	-79		
802.11ac_40MHz	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	MCS0	-88	MCS5	-72
	MCS1	-86	MCS6	-70
	MCS2	-83	MCS7	-69
	MCS3	-80	MCS8	-65
	MCS4	-76	MCS9	-64
802.11ac_80MHz	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	MCS0	-85	MCS5	-68
	MCS1	-82	MCS6	-67
	MCS2	-79	MCS7	-65
	MCS3	-76	MCS8	-62
	MCS4	-73	MCS9	-61

802.11ax_20MHz	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	HE0	-90	HE6	-73
	HE1	-88	HE7	-70
	HE2	-86	HE8	-68
	HE3	-83	HE9	-64
	HE4	-79	HE10	-59
	HE5	-75	HE11	-57
802.11ax_40MHz	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	HE0	-88	HE6	-70
	HE1	-86	HE7	-69
	HE2	-83	HE8	-65
	HE3	-80	HE9	-64
	HE4	-76	HE10	-60
	HE5	-72	HE11	-55
802.11ax_80MHz	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	HE0	-85	HE6	-67
	HE1	-82	HE7	-65
	HE2	-79	HE8	-62
	HE3	-76	HE9	-61
	HE4	-73	HE10	-57
	HE5	-68	HE11	-53
Maximum Input Level	802.11a/n/ac/ax : -30 dBm			

2.4 Bluetooth RF Specification

Conditions: VBAT=3.3V ; VDDIO=1.8V ; Temp:25°C

RF Specification	
Output Power , tolerance ± 1.5 dB	
	CL1 (dBm)
BDR Output Power	6
EDR Output Power	5
BLE Output Power	6
Sensitivity, tolerance ± 1.5 dB	
Sensitivity @ BER=0.1% for GFSK (1Mbps)	-87 dBm
Sensitivity @ BER=0.01% for $\pi/4$ -DQPSK (2Mbps)	-87 dBm
Sensitivity @ BER=0.01% for 8DPSK (3Mbps)	-84 dBm
Sensitivity @ BER=30.8% for LE (1Mbps)	-90 dBm
Sensitivity @ BER=30.8% for 2LE (2Mbps)	-90 dBm
Maximum Input Level	GFSK (1Mbps): -20dBm
	$\pi/4$ -DQPSK (2Mbps): -20dBm
	8DPSK (3Mbps): -20dBm

Note* : The Bluetooth BDR output power is able to be configured by firmware (hcd file).

3. Electrical Characteristics

3.1 Absolute Maximum Ratings

Symbol	Description	Min.	Max.	Unit
VBAT	Input supply Voltage	3.0	5.25	V
VDDIO	Digital/Bluetooth/SDIO/ I/O Voltage	1.62	1.95	V

Note : RF performance is optimal for $3.2V \leq VBAT \leq 5.0V$. For $2.5 V \leq VBAT \leq 3.2V$, device radios will operate but RF performance will degrade.

3.2 Recommended Operating Rating

The module requires two power supplies: VBAT and VDDIO.

Voltage rails	Min.	Typ.	Max.	Unit
VBAT	3.2	3.3	3.8	V
VDDIO	1.62	1.8	1.98	V

VBAT current consumption 1200mA(Peak), when VBAT = 3.3V

The module requires two power supplies: other Digital I/O Pins.

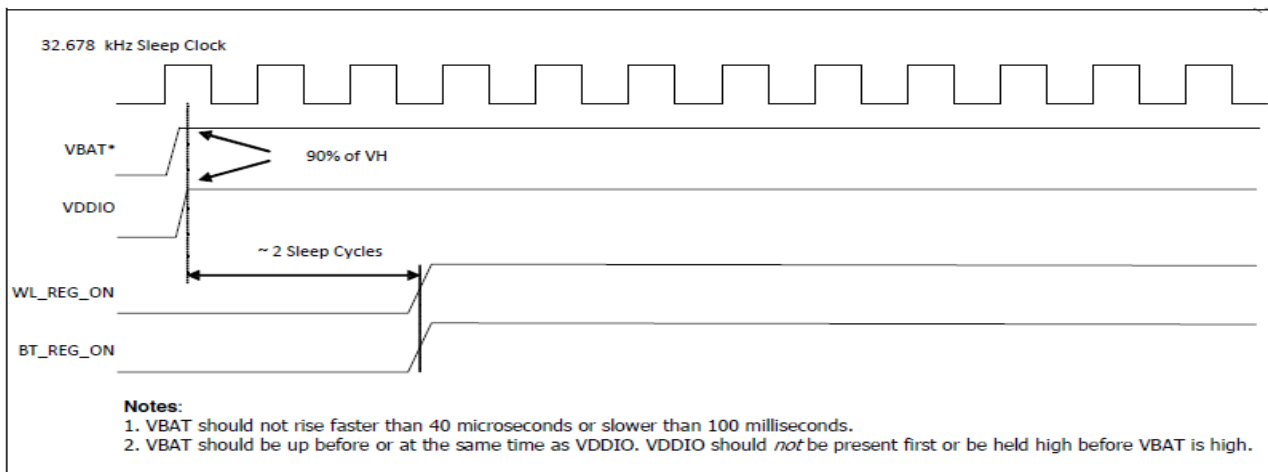
For VDDIO=1.8V	Min.	Max.	Unit
Input high voltage	$0.65 \times VDDIO$	NA	V
Input low voltage	NA	$0.35 \times VDDIO$	V
Output high voltage @ 2mA	$VDDIO - 0.4$	NA	V
Output low voltage @ 2mA	NA	0.4	V

4. Host Interface Timing Diagram

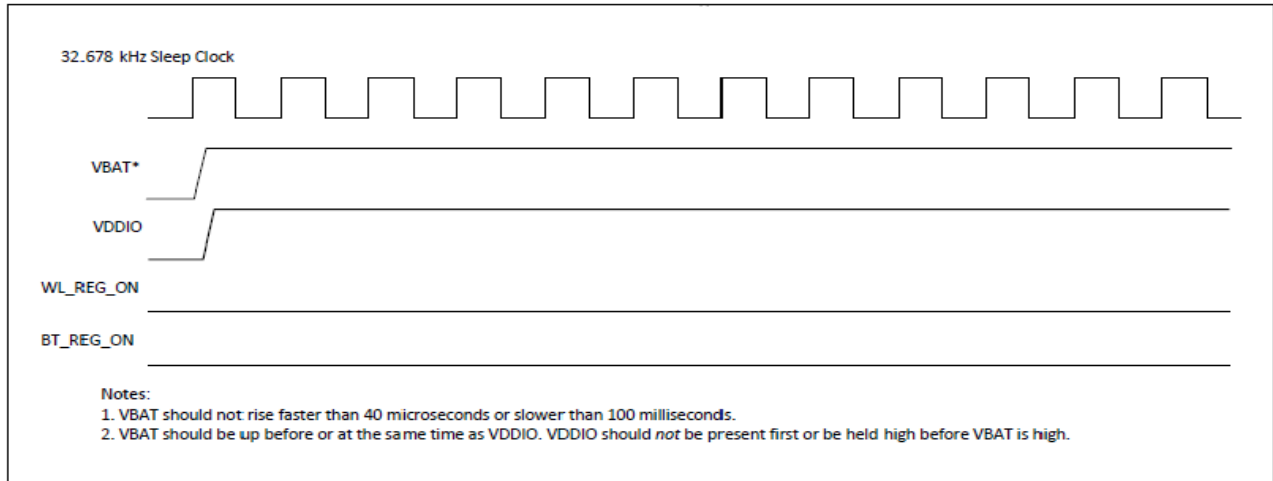
4.1 Power-up Sequence Timing Diagram

The module has signals that allow the host to control power consumption by enabling or disabling the Bluetooth, WLAN and internal regulator blocks. These signals are described below. Additionally, diagrams are provided to indicate proper sequencing of the signals for various operating states. The timing values indicated are minimum required values: longer delays are also acceptable.

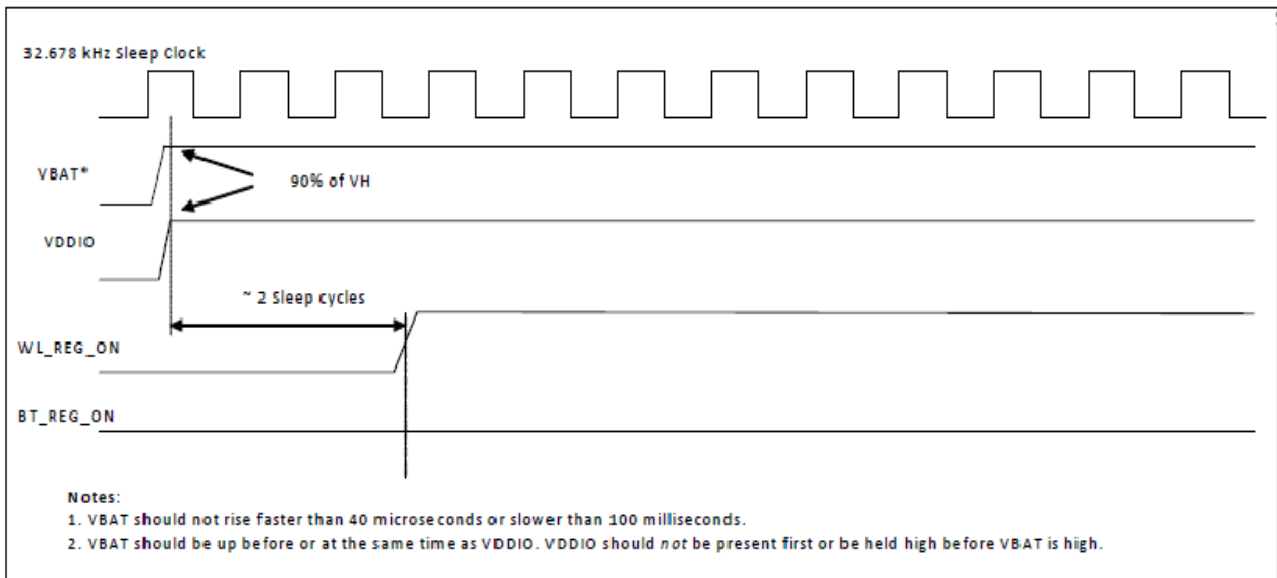
- **WL_REG_ON:** Used by the PMU to power up or power down the internal regulators used by the WLAN section. When this pin is high, the regulators are enabled and the WLAN section is out of reset. When this pin is low the WLAN section is in reset.
- **BT_REG_ON:** Used by the PMU to power up or power down the internal regulators used by the BT section. Low asserting reset for Bluetooth. This pin has no effect on WLAN and does not control any PMU functions. This pin must be driven high or low (not left floating).



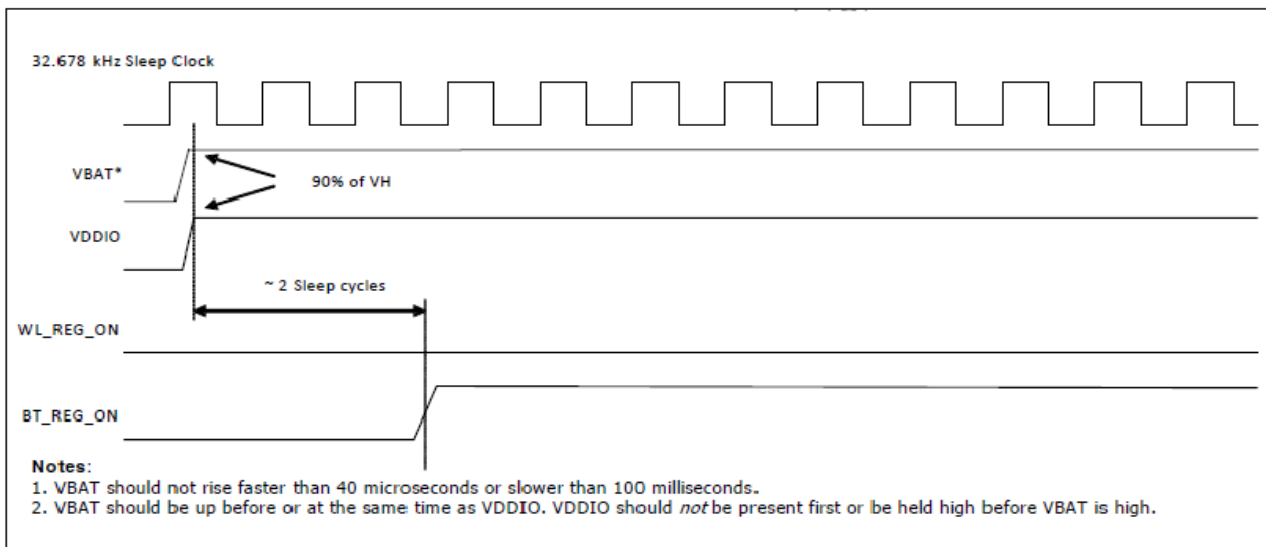
WLAN=ON, Bluetooth=ON



WLAN=OFF, Bluetooth=OFF

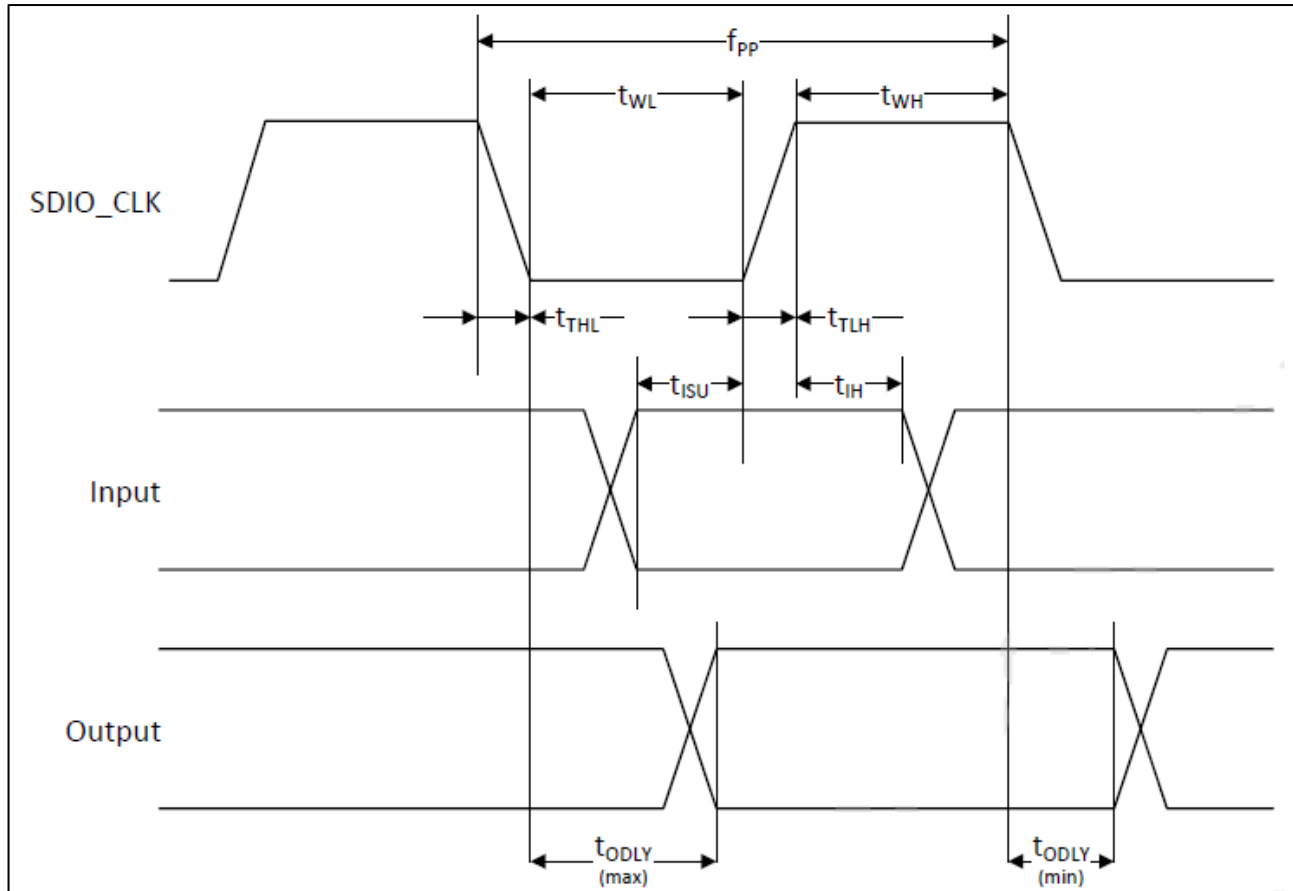


WLAN=ON, Bluetooth=OFF



WLAN=OFF, Bluetooth=ON

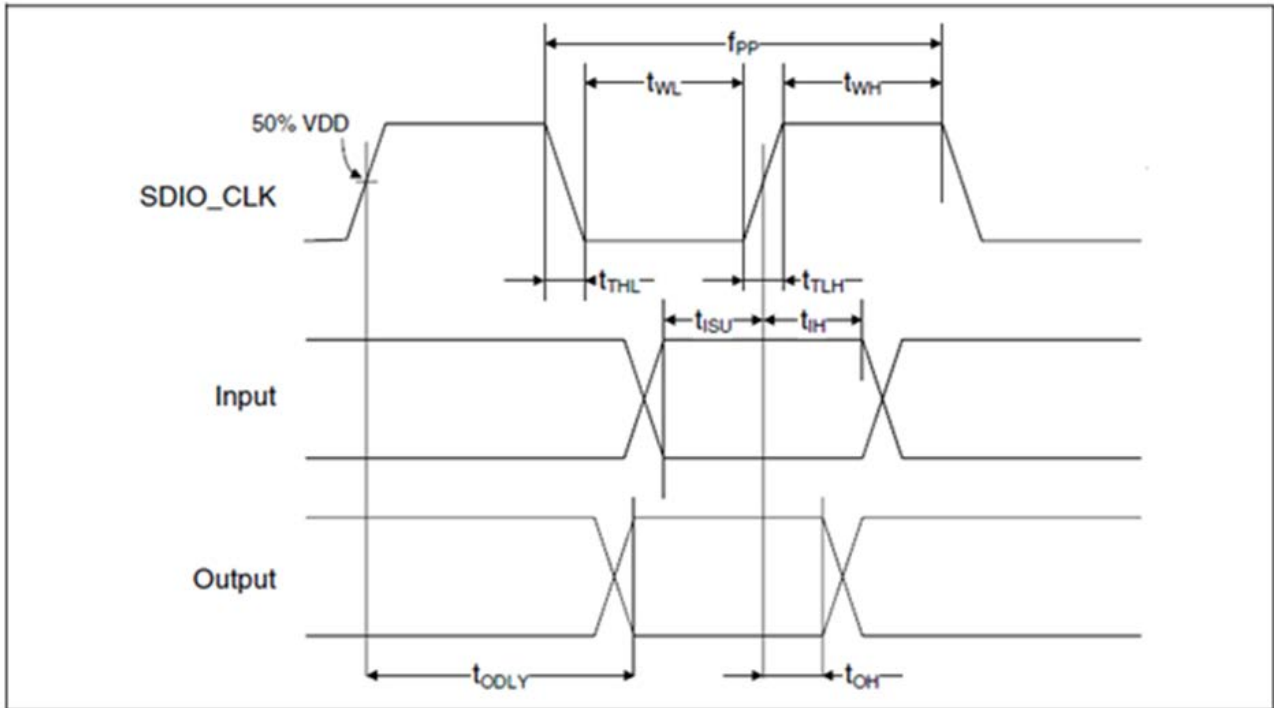
4.2 SDIO Default Mode Timing Diagram



Parameter	Symbol	Minimum	Typical	Maximum	Unit
SDIO CLK (ALL values are referred to minimum VIH and maximum VIL b)					
Frequency – Data Transfer mode	f_{PP}	0	-	25	MHz
Frequency – Identification mode	f_{OD}	0	-	400	kHz
Clock low time	t_{WL}	10	-	-	ns
Clock high time	t_{WH}	10	-	-	ns
Clock rise time	t_{TLH}	-	-	10	ns
Clock low time	t_{THL}	-	-	10	ns
Inputs : CMD, DAT(referenced to CLK)					
Input setup time	t_{ISU}	5	-	-	ns
Input hold time	t_{IH}	5	-	-	ns
Outputs : CMD, DAT(referenced to CLK)					
Output delay time, - Data Transfer mode	t_{ODLY}	0	-	14	ns
Output delay time, - Identification mode	t_{ODLY}	0	-	50	ns

- Timing is based on $CL \leq 40$ pF load on CMD and Data.
- Min. (V_{IH}) = $0.7 \times V_{DDIO}$ and max. (V_{IL}) = $0.2 \times V_{DDIO}$

4.3 SDIO High Speed Mode Timing Diagram

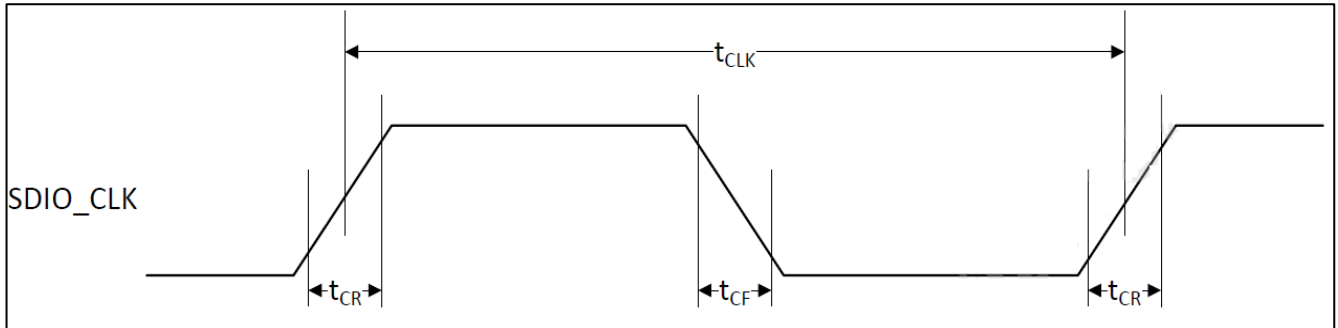


Parameter	Symbol	Minimum	Typical	Maximum	Unit
SDIO CLK (ALL values are referred to minimum VIH and maximum VIL^b)					
Frequency – Data Transfer mode	f_{PP}	0	-	50	MHz
Frequency – Identification mode	f_{OD}	0	-	400	kHz
Clock low time	t_{WL}	7	-	-	ns
Clock high time	t_{WH}	7	-	-	ns
Clock rise time	t_{TLH}	-	-	3	ns
Clock low time	t_{THL}	-	-	3	ns
Inputs : CMD, DAT(referenced to CLK)					
Input setup time	t_{ISU}	6	-	-	ns
Input hold time	t_{IH}	2	-	-	ns
Outputs : CMD, DAT(referenced to CLK)					
Output delay time - Data Transfer mode	t_{ODLY}	-	-	14	ns
Output hold time	t_{OH}	2.5	-	-	ns
Total system capacitance(each line)	C_L			40	pF

- Timing is based on $C_L \leq 40$ pF load on CMD and Data.
- Min. (Vih) = 0.7 x VDDIO and max. (Vil) = 0.2 x VDDIO

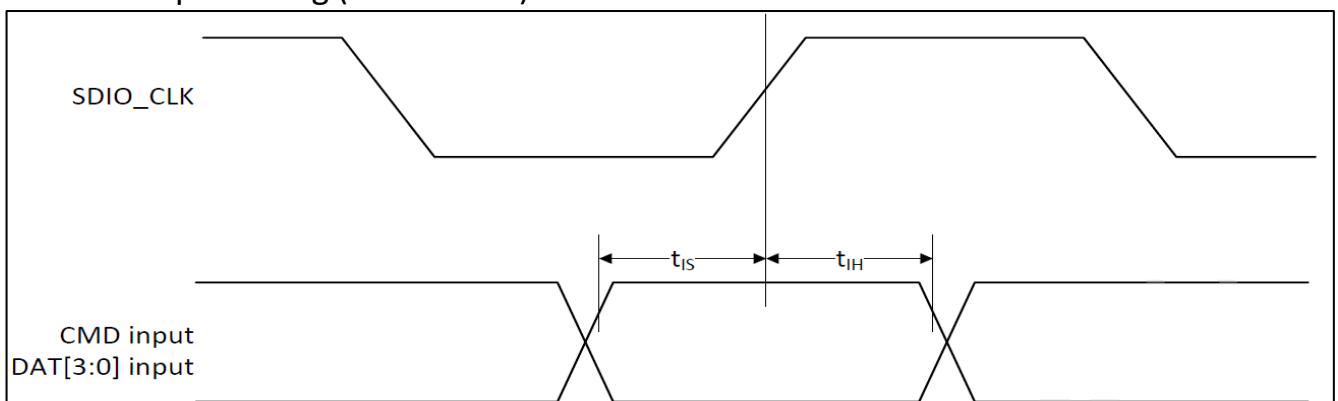
4.4 SDIO Bus Timing Specifications in SDR Modes

Clock timing (SDR Modes)



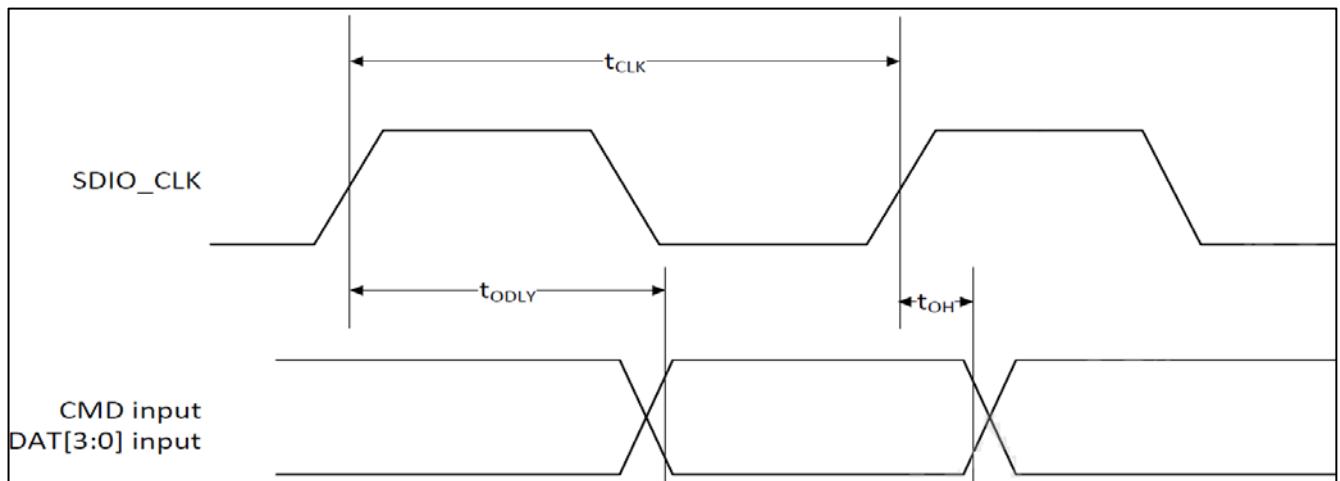
Parameter	Symbol	Minimum	Maximum	Unit	Comments
-	t_{CLK}	40	-	ns	SDR12 mode
		20	-	ns	SDR25mode
		10	-	ns	SDR50 mode
		4.8	-	ns	SDR104 mode
-	t_{CR}, t_{CF}	-	$0.2 \times t_{CLK}$	ns	$t_{CR}, t_{CF} < 2.00$ ns (max) @100MHz, $C_{CARD} = 10$ pF $t_{CR}, t_{CF} < 0.96$ ns (max) @208MHz, $C_{CARD} = 10$ pF
Clock duty	-	30	70	%	-

SDIO Bus Input timing (SDR Modes)



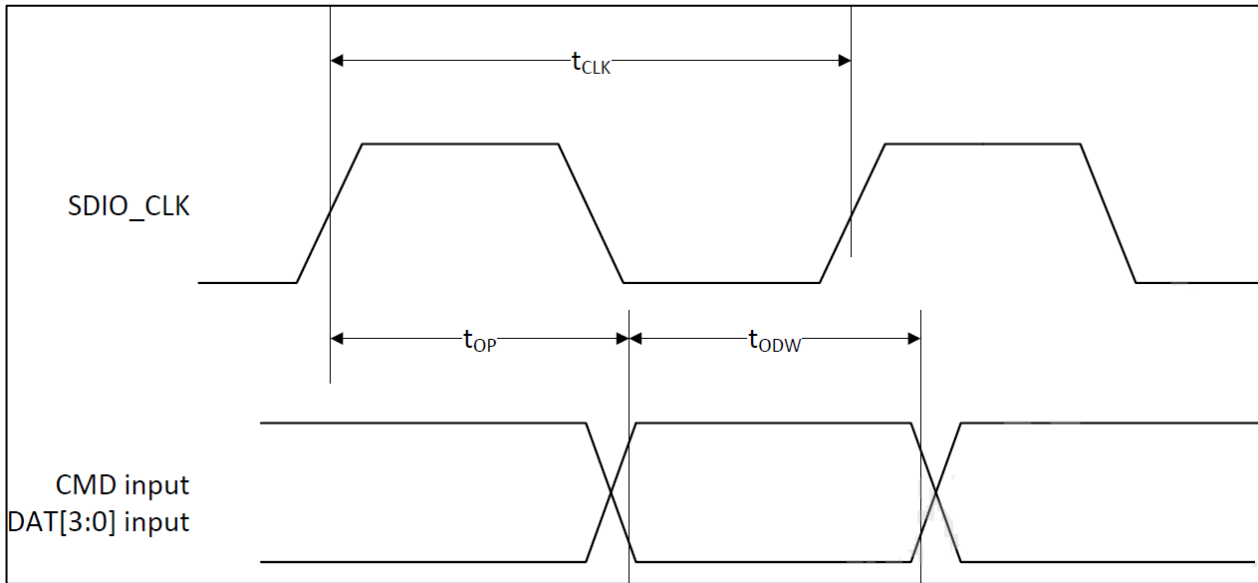
Symbol	Minimum	Maximum	Unit	Comments
SDR104 Mode				
t_{IS}	1.4	-	ns	$C_{CARD} = 10 \text{ pF}$, $V_{CT} = 0.975V$
t_{IH}	0.80	-	ns	$C_{CARD} = 5 \text{ pF}$, $V_{CT} = 0.975V$
SDR50 Mode				
t_{IS}	3.00	-	ns	$C_{CARD} = 10 \text{ pF}$, $V_{CT} = 0.975V$
t_{IH}	0.80	-	ns	$C_{CARD} = 5 \text{ pF}$, $V_{CT} = 0.975V$

SDIO Bus output timing (SDR Modes up to 100MHz)



Symbol	Minimum	Maximum	Unit	Comments
t_{ODLY}	-	7.5	ns	$t_{CLK} \geq 10 \text{ ns}$ $C_L = 30 \text{ pF}$ using driver type B for SDR50
t_{ODLY}	-	14.0	ns	$t_{CLK} \geq 20 \text{ ns}$ $C_L = 40 \text{ pF}$ using for SR12, SDR25
t_{OH}	1.5	-	ns	Hold time at the t_{ODLY} (min) $C_L = 15 \text{ pF}$

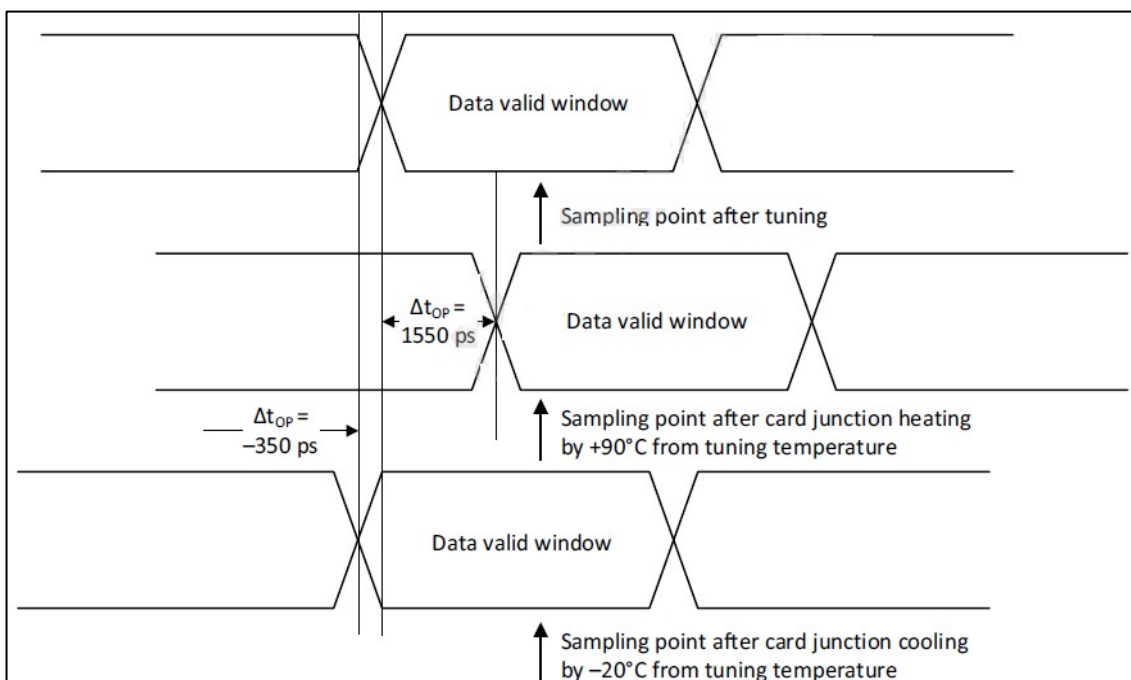
Card output timing (SDR Modes 100MHz to 208MHz)



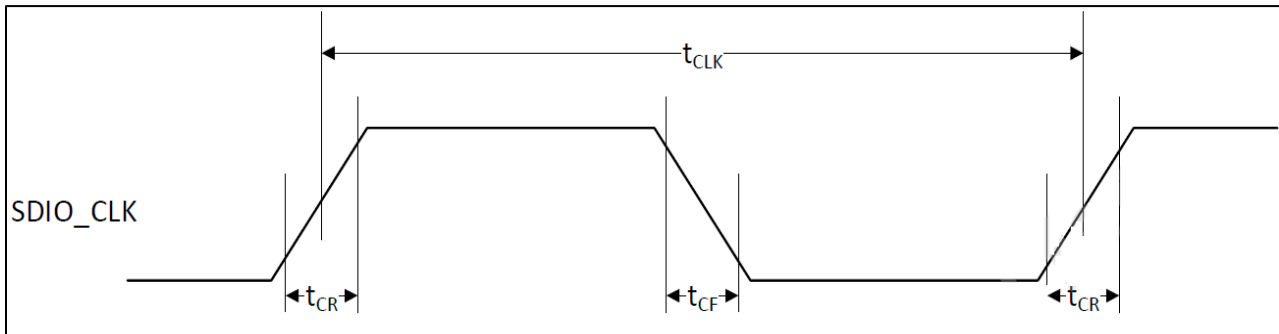
Symbol	Minimum	Maximum	Unit	Comments
t_{OP}	0	2	UI	Card output phase
Δt_{OP}	-350	+1550	ps	Delay variation due to temp. change after tuning
Δt_{ODW}	0.60	-	UI	$t_{ODW} = 2.88 \text{ ns @ } 208\text{MHz}$

- $\Delta t_{OP} = +1550 \text{ ps}$ for junction temperature of $\Delta t_{OP} = 90$ degrees during operation
- $\Delta t_{OP} = -350 \text{ ps}$ for junction temperature of $\Delta t_{OP} = -20$ degrees during operation
- $\Delta t_{OP} = +2600 \text{ ps}$ for junction temperature of $\Delta t_{OP} = -20$ to $+125$ degrees during operation

Δt_{OP} Consideration for Variable Data Window (SDR 104 Mode)

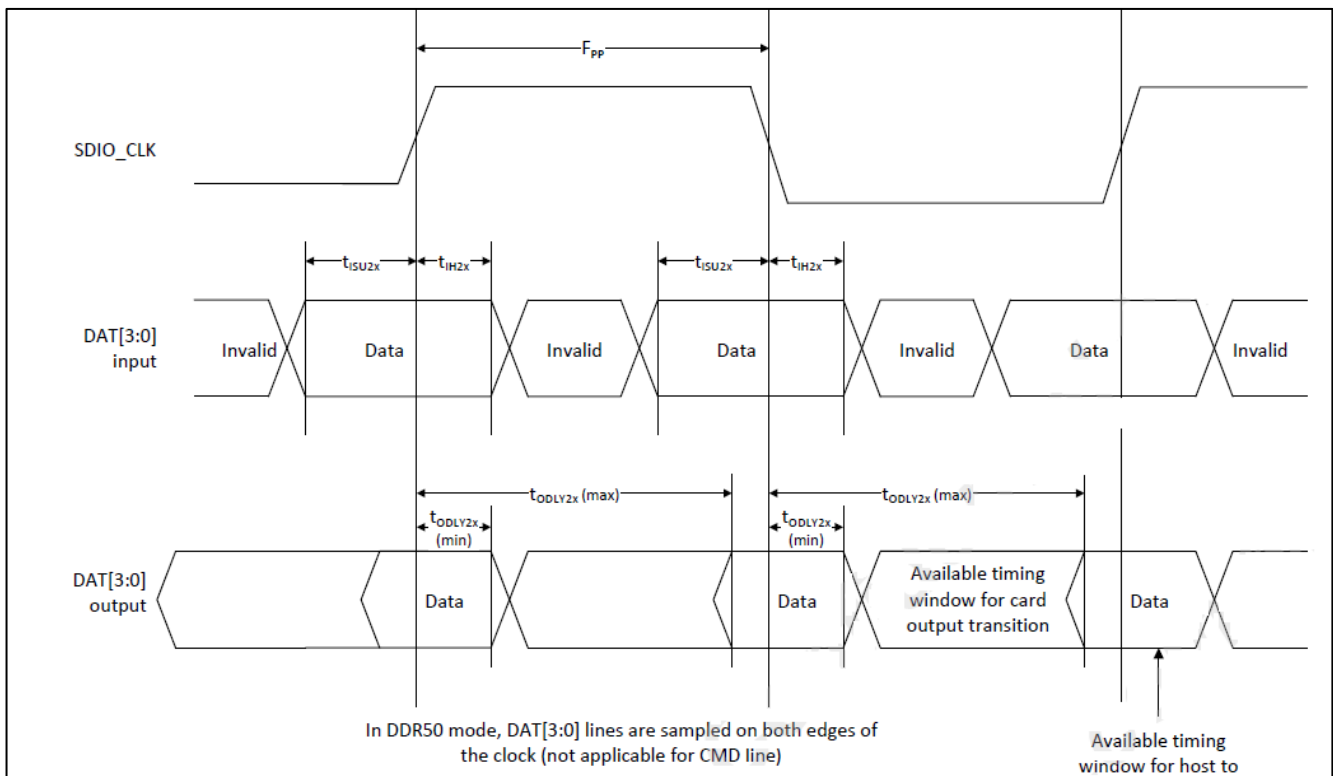


4.5 SDIO Bus Timing Specifications in DDR50 Mode



Parameter	Symbol	Minimum	Maximum	Unit	Comments
-	t_{CLK}	20	-	ns	DDR50 mode
-	t_{CR}, t_{CF}	-	$0.2 \times t_{CLK}$	ns	$t_{CR}, t_{CF} < 4.00 \text{ ns(max) @ 50MHz}$ $C_{CARD} = 10 \text{ pF}$
Clock duty	-	45	55	%	-

Data Timing



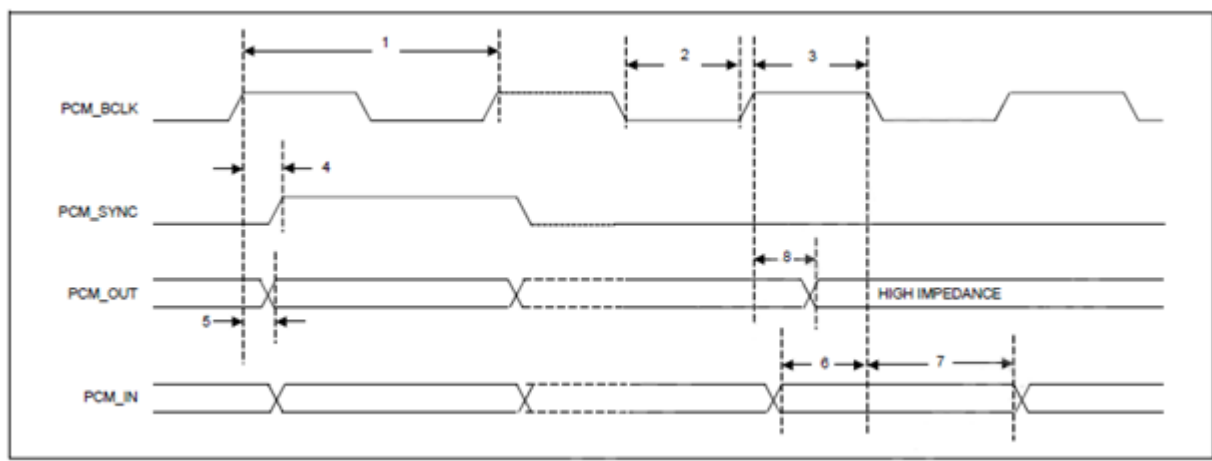
Parameter	Symbol	Minimum	Maximum	Unit	Comments
Input CMD					
Input setup time	t_{ISU}	6	-	ns	$C_{CARD} < 10 \text{ pF}$ (1 Card)
Input hold time	t_{IH}	0.8	-	ns	$C_{CARD} < 10 \text{ pF}$ (1 Card)
Output CMD					
Output delay time	t_{ODLY}	-	13.7	ns	$C_{CARD} < 30 \text{ pF}$ (1 Card)
Output hold time	t_{OH}	1.5	-	ns	$C_{CARD} < 15 \text{ pF}$ (1 Card)
Input DAT					
Input setup time	t_{ISU2x}	3	-	ns	$C_{CARD} < 10 \text{ pF}$ (1 Card)
Input hold time	t_{IH2x}	0.8	-	ns	$C_{CARD} < 10 \text{ pF}$ (1 Card)
Output DAT					
Output delay time	t_{ODLY2x}	-	7.5	ns	$C_{CARD} < 25 \text{ pF}$ (1 Card)
Output hold time	t_{ODLY2x}	1.5	-	ns	$C_{CARD} < 15 \text{ pF}$ (1 Card)

4.6 PCM Interface Description

The PCM Interface on the AP6281 can connect to linear PCM Codec devices in master or slave mode. In master mode, the AP6281 generates the PCM_CLK and PCM_SYNC signals, and in slave mode, these signals are provided by another master on the PCM interface and are inputs to the AP6281. The configuration of the PCM interface may be adjusted by the host through the use of vendor-specific HCI commands.

Short Frame Sync, Master Modem

PCM Timing Diagram (Short Frame Sync, Master Mode)

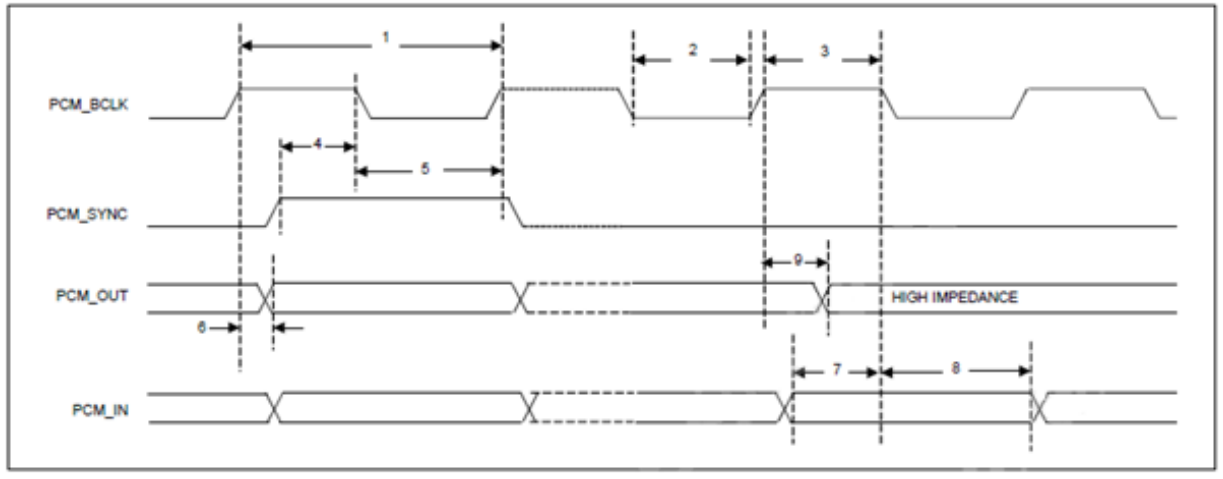


PCM Interface Timing Specifications (Short Frame Sync, Master Mode)

Reference	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency		-	12	MHz
2	PCM bit clock low	41	-	-	ns
3	PCM bit clock high	41	-	-	ns
4	PCM_SYNC delay	0	-	25	ns
5	PCM_OUT delay	0	-	25	ns
6	PCM_IN setup	8	-	-	ns
7	PCM_IN hold	8	-	-	ns
8	Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance	0	-	25	ns

Short Frame Sync, Slave Mode

PCM Timing Diagram (Short Frame Sync, Slave Mode)

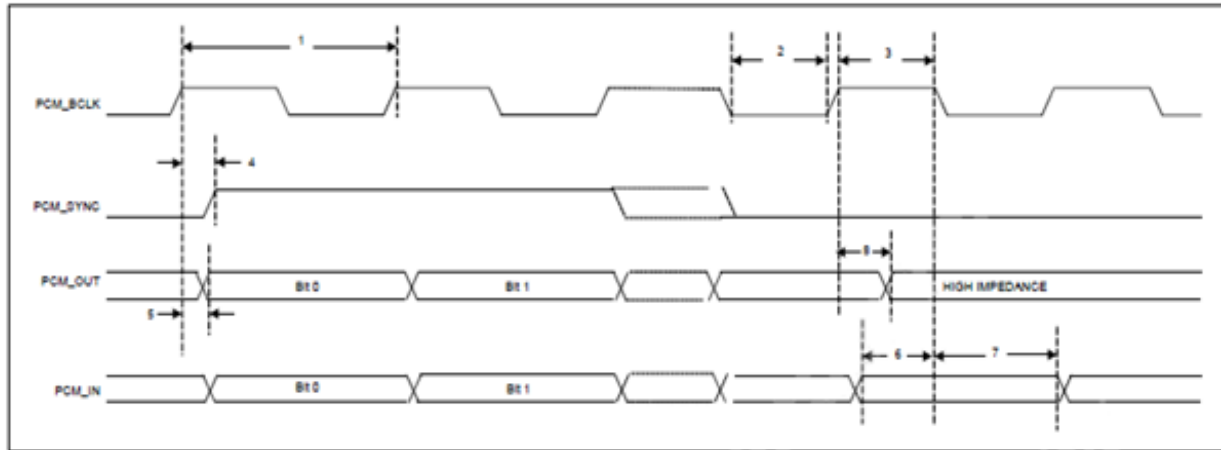


PCM Interface Timing Specifications (Short Frame Sync, Slave Mode)

Reference	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency		-	12	MHz
2	PCM bit clock low	41	-	-	ns
3	PCM bit clock high	41	-	-	ns
4	PCM_SYNC setup	8	-	-	ns
5	PCM_SYNC hold	8	-	-	ns
6	PCM_OUT delay	0	-	25	ns
7	PCM_IN setup	8	-	-	ns
8	PCM_IN hold	8	-	-	ns
9	Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance	0	-	25	ns

Long Frame Sync, Master Mode

PCM Timing Diagram (Long Frame Sync, Master Mode)

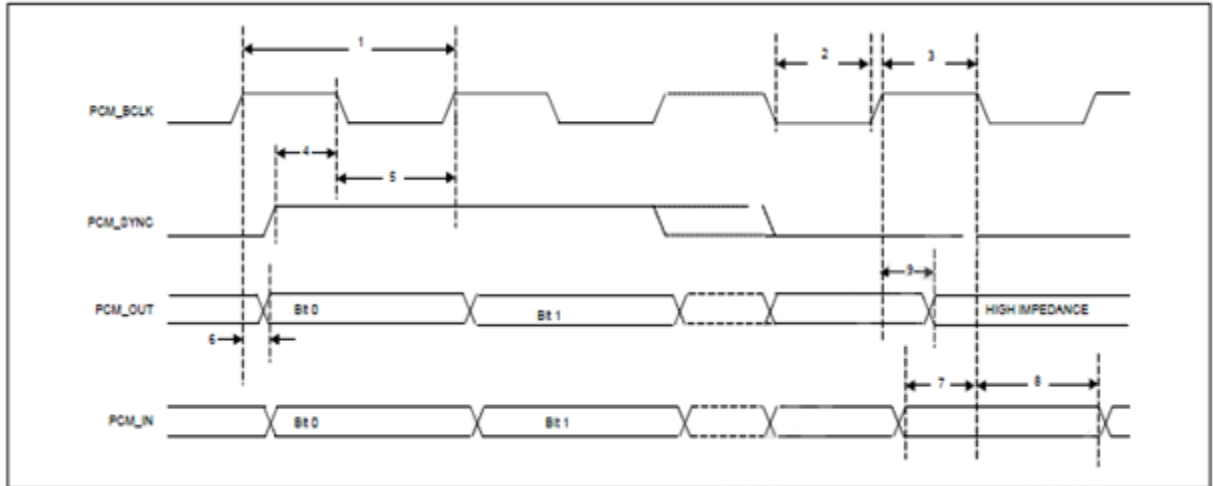


PCM Interface Timing Specifications (Long Frame Sync, Master Mode)

Reference	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency		-	12	MHz
2	PCM bit clock low	41	-	-	ns
3	PCM bit clock high	41	-	-	ns
4	PCM_SYNC delay	0	-	25	ns
5	PCM_OUT delay	0	-	25	ns
6	PCM_IN setup	8	-	-	ns
7	PCM_IN hold	8	-	-	ns
8	Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance	0	-	25	ns

Long Frame Sync, Slave Mode

PCM Timing Diagram (Long Frame Sync, Slave Mode)

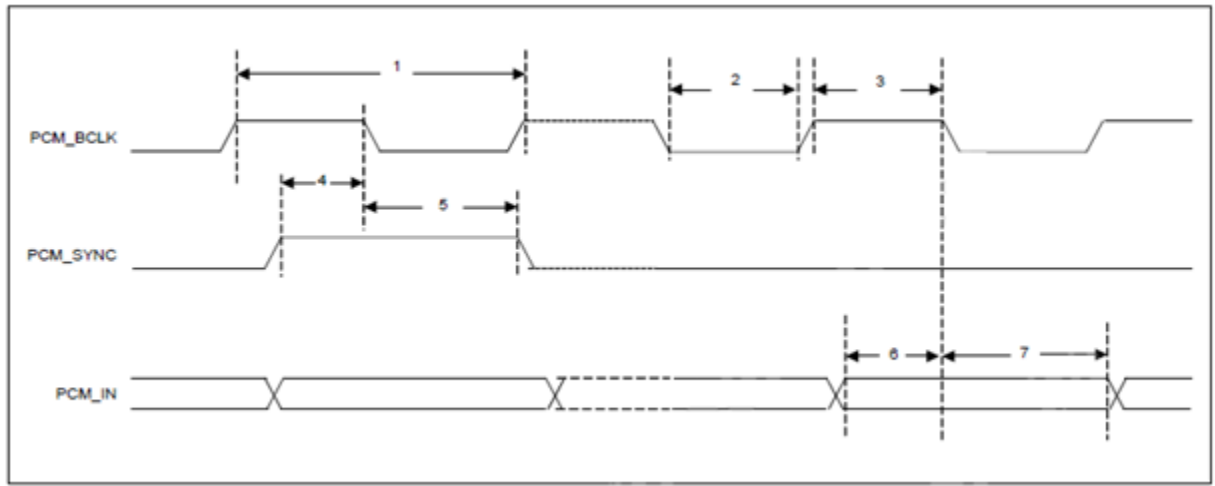


PCM Interface Timing Specifications (Long Frame Sync, Slave Mode)

Reference	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency		-	12	MHz
2	PCM bit clock low	41	-	-	ns
3	PCM bit clock high	41	-	-	ns
4	PCM_SYNC setup	8	-	-	ns
5	PCM_SYNC hold	8	-	-	ns
6	PCM_OUT delay	0	-	25	ns
7	PCM_IN setup	8	-	-	ns
8	PCM_IN hold	8	-	-	ns
9	Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance	0	-	25	ns

Short Frame Sync, Burst Mode

PCM Burst Mode Timing (Receive Only, Short Frame Sync)

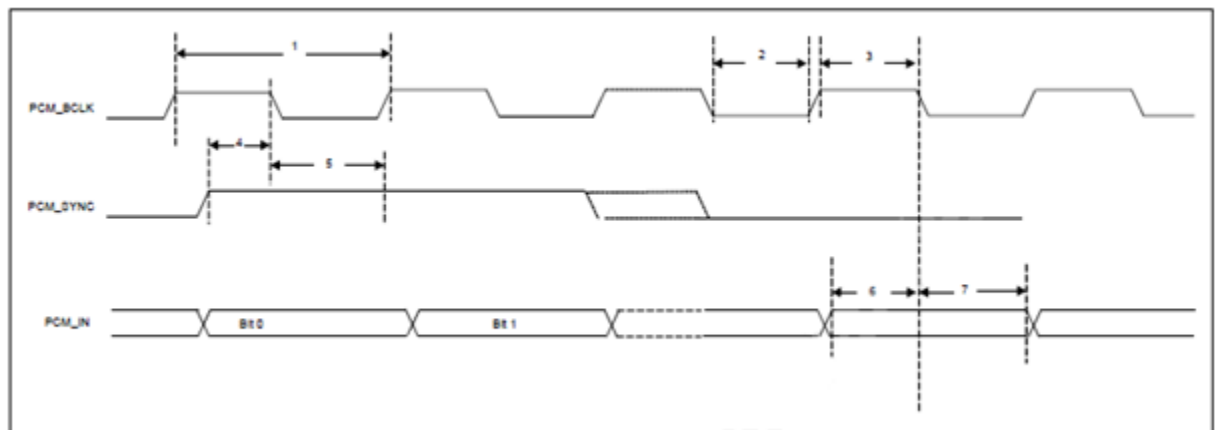


PCM Burst Mode (Receive Only, Short Frame Sync)

Reference	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency	-	-	24	MHz
2	PCM bit clock low	20.8	-	-	ns
3	PCM bit clock high	20.8	-	-	ns
4	PCM_SYNC setup	8	-	-	ns
5	PCM_SYNC hold	8	-	-	ns
6	PCM_IN setup	8	-	-	ns
7	PCM_IN hold	8	-	-	ns

Long Frame Sync, Burst Mode

PCM Burst Mode Timing (Receive Only, Long Frame Sync)



PCM Burst Mode (Receive Only, Long Frame Sync)

Reference	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency	-	-	24	MHz
2	PCM bit clock low	20.8	-	-	ns
3	PCM bit clock high	20.8	-	-	ns
4	PCM_SYNC setup	8	-	-	ns
5	PCM_SYNC hold	8	-	-	ns
6	PCM_IN setup	8	-	-	ns
7	PCM_IN hold	8	-	-	ns

4.7 UART Interface Description

The UART is a standard 4-wire interface (RX, TX, RTS, and CTS) with adjustable baud rates from 9600 bps to 4.0 Mbps. The interface features an automatic baud rate detection capability that returns a baud rate selection. Alternatively, the baud rate may be selected through a vendor-specific UART HCI command.

UART has a 1040-byte receive FIFO and a 1040-byte transmit FIFO to support EDR. Access to the FIFOs is conducted through the AHB interface through either DMA or the CPU. The UART supports the Bluetooth 5.0 UART HCI specification: H4, a custom Extended H4, and H5. The default baud rate is 115.2 Kbaud.

The UART supports the 3-wire H5 UART transport, as described in the Bluetooth specification (Three-wire UART Transport Layer). Compared to H4, the H5 UART transport reduces the number of signal lines required by eliminating the CTS and RTS signals.

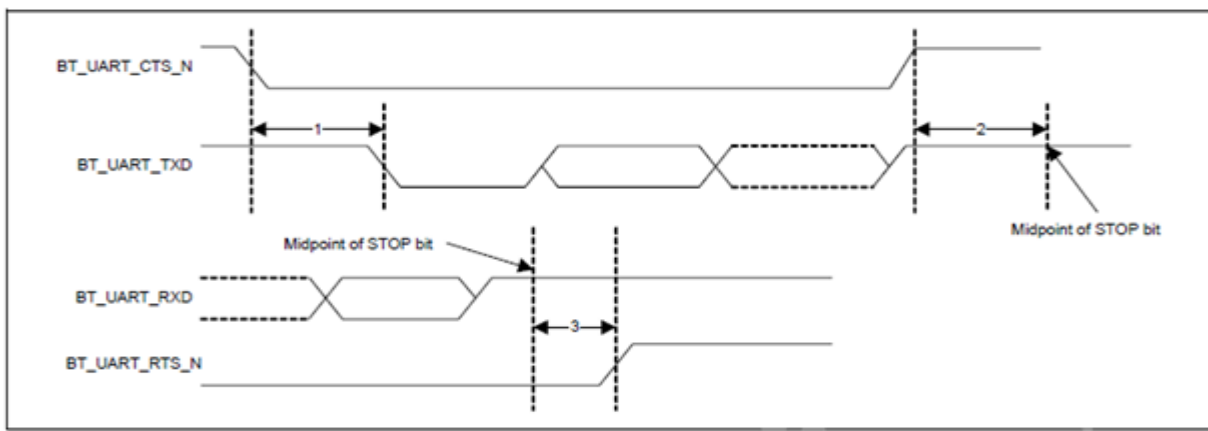
The UART can perform XON/XOFF flow control and includes hardware support for the Serial Line Input Protocol (SLIP). It can also perform wake-on activity. For example, activity on the RX or CTS inputs can wake the chip from a sleep state.

Normally, the UART baud rate is set by a configuration record downloaded after device reset, or by automatic baud rate detection, and the host does not need to adjust the baud rate. Support for changing the baud rate during normal HCI UART operation is included through a vendor-specific command that allows the host to adjust the contents of the baud rate registers. The UARTs operate correctly with the host UART as long as the combined baud rate error of the two devices is within $\pm 2\%$.

Example of Common Baud Rates

Desired Rate	Actual Rate	Error(%)
4000000	4000000	0.00
3692000	3692308	0.01
3000000	3000000	0.00
2000000	2000000	0.00
1500000	1500000	0.00
1444444	1454544	0.70
921600	923077	0.16
460800	461538	0.16
230400	230796	0.17
115200	115385	0.16
57600	57692	0.16
38400	38400	0.00
28800	28846	0.16
19200	19200	0.00
14400	14423	0.16
9600	9600	0.00

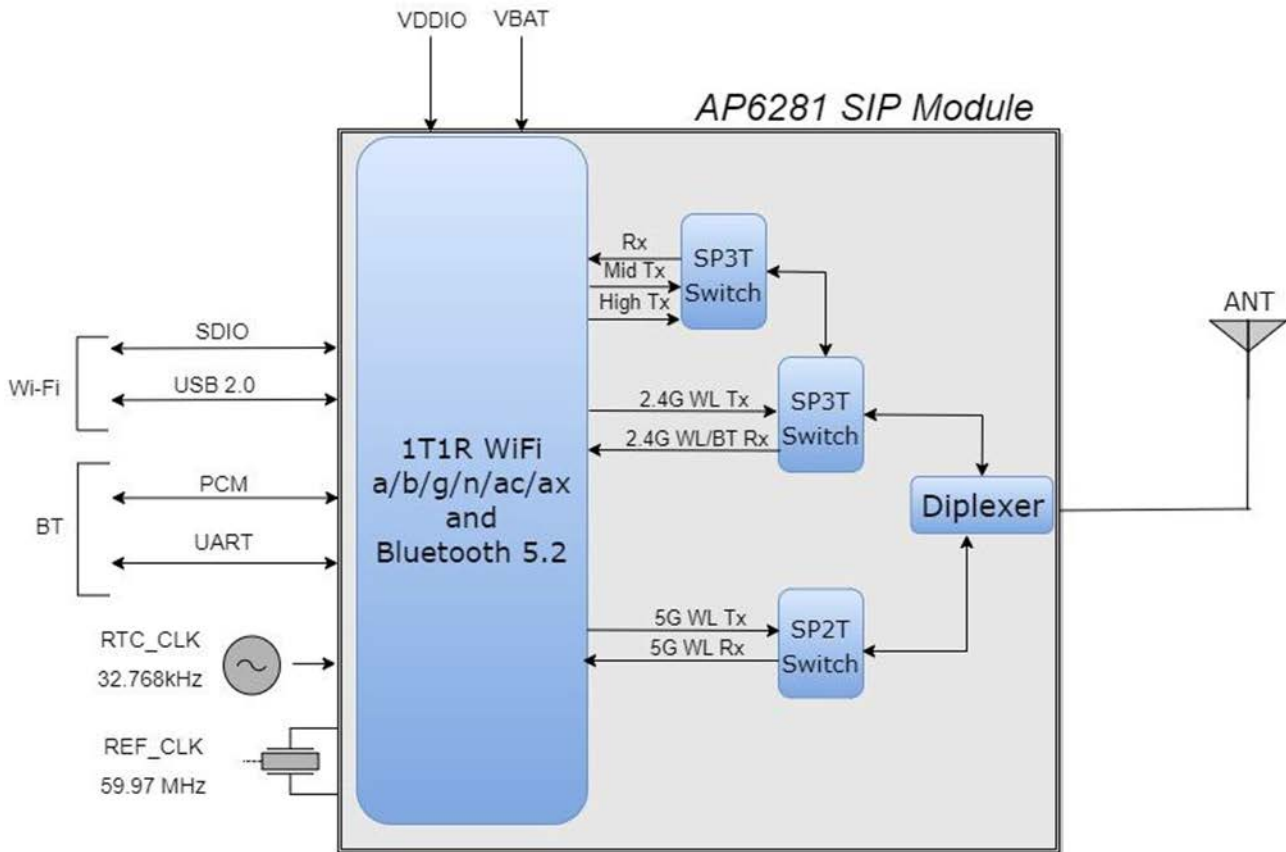
UART Timing



UART Timing Specifications

Ref	Characteristics	Min.	Typ.	Max.	Unit
1	Delay time, BT_UART_CTS_N low BT_UART_TXD valid	-	-	1.5	Bit periods
2	Setup time, BT_UART_CTS_N high before midpoint of stop bit	-	-	0.5	Bit periods
3	Delay time, midpoint of stop bit BT_UART_RTS_N high	-	-	0.5	Bit periods

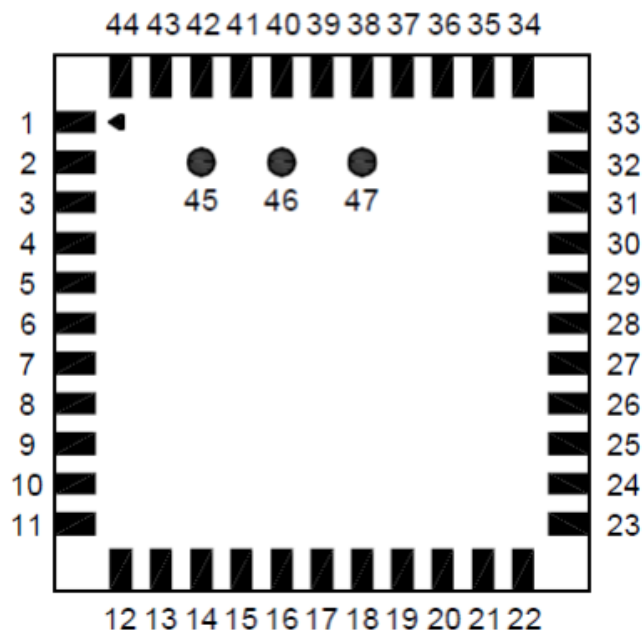
5. Block Diagram



6. Pin Definition

6.1 Pin Outline

<TOP VIEW>



6.2 Pin Table

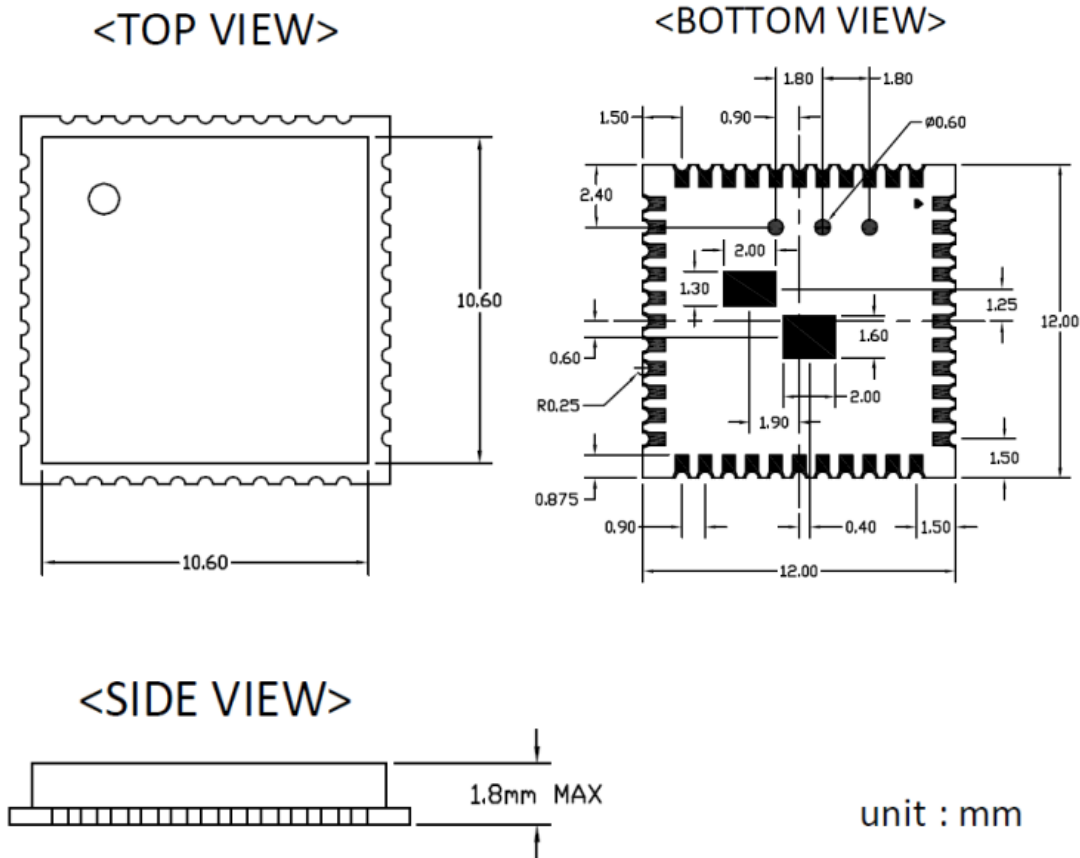
NO	Name	Type	Description
1	GND	—	Ground connections
2	WL_BT_ANT	I/O	RF I/O port
3	GND	—	Ground connections
4	WL_GPIO_1	I/O	This pin can be programmed to be a GPIO, or the GCI external coexistence interface.
5	WL_GPIO_2	I/O	This pin can be programmed to be a GPIO, or the GCI external coexistence interface.
6	BT_WAKE	I	HOST wake-up Bluetooth device
7	BT_HOST_WAKE	O	Bluetooth device to wake-up HOST
8	WL_GPIO_3	I/O	This pin can be programmed to be a GPIO, or the GCI external coexistence interface.
9	VBAT	P	Main power voltage source input
10	XTAL_IN	I	Crystal input

11	XTAL_OUT	O	Crystal output
12	WL_REG_ON	I	Power up/down internal regulators used by WiFi section
13	WL_HOST_WAKE	O	WLAN to wake-up HOST
14	SDIO_DATA_2	I/O	SDIO data line 2
15	SDIO_DATA_3	I/O	SDIO data line 3
16	SDIO_DATA_CMD	I/O	SDIO command line
17	SDIO_DATA_CLK	I/O	SDIO clock line
18	SDIO_DATA_0	I/O	SDIO data line 0
19	SDIO_DATA_1	I/O	SDIO data line 1
20	GND	—	Ground connections
21	ASR_VLX	O	Internal Analog Buck voltage generation pin
22	VDDIO	P	I/O Voltage supply input
23	ABUCK_1P12	I	Internal Analog Buck voltage generation pin
24	LPO	I	External Low Power Clock input (32.768KHz)
25	PCM_OUT	O	PCM Data output
26	PCM_CLK	I/O	PCM clock
27	PCM_IN	I	PCM data input
28	PCM_SYNC	I/O	PCM sync signal
29	WL_GPIO_19	I/O	This pin can be programmed to be a GPIO, or the GCI external coexistence interface.
30	WL_GPIO_20	I/O	This pin can be programmed to be a GPIO, or the GCI external coexistence interface.
31	GND	—	Ground connections
32	USB 5V	—	USB 5V signal. Isolate the pin32 using an external resistor so that the USB pin sees a lower voltage. If USB is not used, leave it floating.
33	GND	—	Ground connections
34	BT_REG_ON	I	Power up/down internal regulators used by BT section
35	WL_GPIO_4	I/O	This pin can be programmed to be a GPIO, or the GCI external coexistence interface.

36	GND	—	Ground connections
37	USB_DP	I/O	USB Data +
38	USB_DM	I/O	USB Data -
39	LHL_XTALI	I/O	32kHz XTAL input
40	LHL_XTALO	I/O	32kHz XTAL output
41	UART_RTS_N	O	Bluetooth UART interface
42	UART_TXD	O	Bluetooth UART interface
43	UART_RXD	I	Bluetooth UART interface
44	UART_CTS_N	I	Bluetooth UART interface
45	BT_GPIO_2	I/O	This pin can be programmed to be a GPIO, or the GCI external coexistence interface.
46	BT_GPIO_3	I/O	This pin can be programmed to be a GPIO, or the GCI external coexistence interface.
47	BT_GPIO_4	I/O	This pin can be programmed to be a GPIO, or the GCI external coexistence interface.

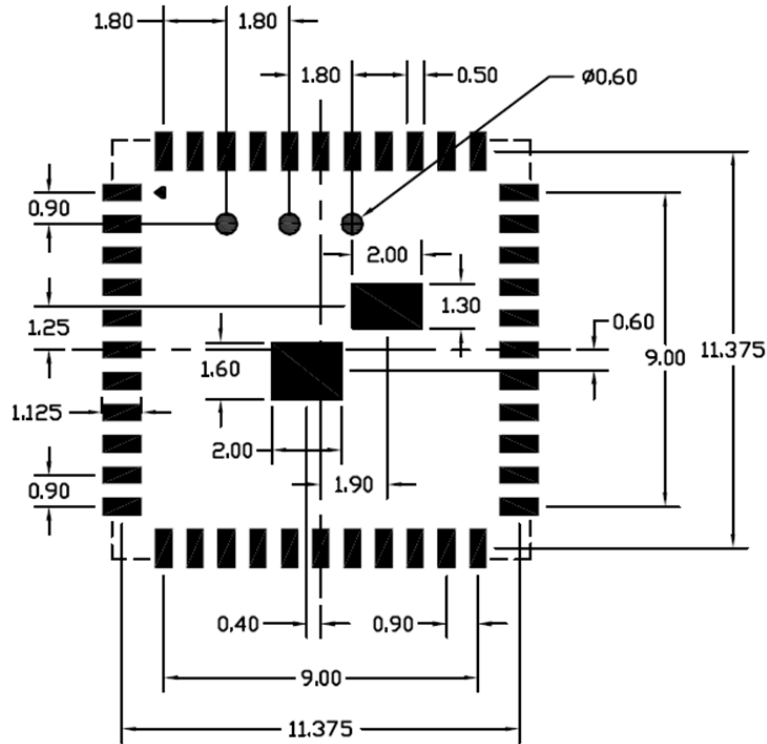
7. Mechanical Specifications

7.1 Module Dimensions



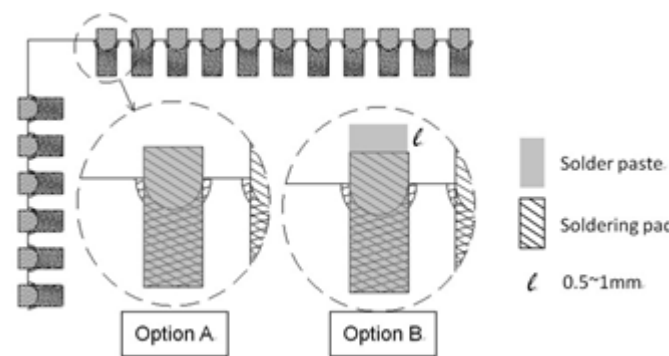
7.2 PCB Footprint

<TOP VIEW>



unit : mm

- Solder paste layer design is generally the same as recommended footprint
If soldering quality with good wetting on upright side is essential for PQC, how to optimize the aperture design in the stencil to adjust the amount of solder paste would be crucial.
In addition, a kind of stencil design with stepped thickness in partial area would be considered if the thickness of stencil is about 0.1mm or thinner. Please optimize the stencil design by manufacture engineer or contact SparkLAN FAE for assistance.



8. External clock reference

External LPO signal characteristics

Parameter	Specification	Units
Nominal input frequency	32.768	kHz
Frequency accuracy	+/-25	ppm
Duty cycle	30 - 70	%
Input signal amplitude	1.8±0.09	V
Signal type	Square-wave or sine-wave	-
Input impedance	>100k <5	Ω pF
Clock jitter (integrated over 300Hz – 15KHz)	<1	Hz
Output high voltage	0.7V _{io} - V _{io}	V

External 37.4MHz X'TAL characteristics

Parameter	Specification	Units
Nominal input frequency – F ₀	59.97	MHz
Frequency Tolerance - $\Delta F / F_0$ (At 25°C +/- 3°C)	+/- 7	ppm
Operation Temperature Range - Topr	-30 ~ + 85	°C
Freq. Stability(over operating temperature) - TC Ref. to 25°C	+/- 10	ppm
Load capacitance - CL	8	pF
Equivalent Series Resistance – ESR	Max. 50	Ω
Drive Level - DL	Typ. 50, Max. 100	uW
Insulation resistance – IR At 100Vdc	Min. 500	MΩ

8.1 SDIO Interface Description

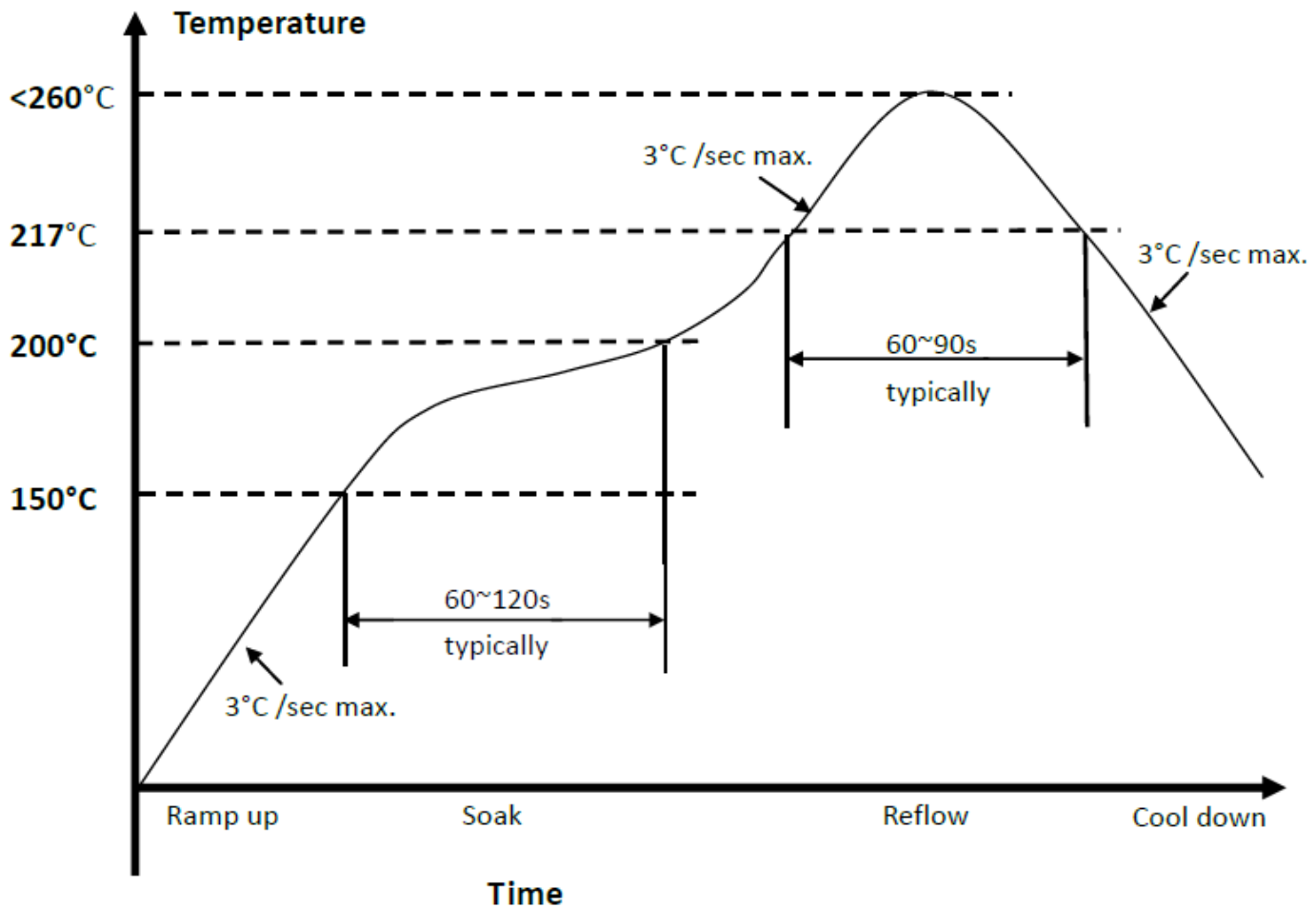
The module supports SDIO version 3.0 for all 1.8V 4-bit UHSI speeds: SDR50 (100 Mbps), SDR104 (208MHz) and DDR50 (50MHz, dual rates), and backward compatible to SDIO version 2.0 default speed (25MHz) and high speed (50 MHz). It has the ability to stop the SDIO clock and map the interrupt signal into a GPIO pin. This ‘out-of-band’ interrupt signal notifies the host when the WLAN device wants to turn on the SDIO interface. The ability to force the control of the gated clocks from within the WLAN chip is also provided.

- Function 0 Standard SDIO function (Max BlockSize / ByteCount = 32B)
- Function 1 Backplane Function to access the internal System On Chip (SOC) address space (Max BlockSize / ByteCount = 64B)
- Function 2 WLAN Function for efficient WLAN packet transfer through DMA (Max BlockSize/ByteCount=512B)

SDIO Pin Description

SD 4-Bit Mode	
DATA0	Data Line 0
DATA1	Data Line 1 or Interrupt
DATA2	Data Line 2 or Read Wait
DATA3	Data Line 3
CLK	Clock
CMD	Command Line

9. Recommended Reflow Profile



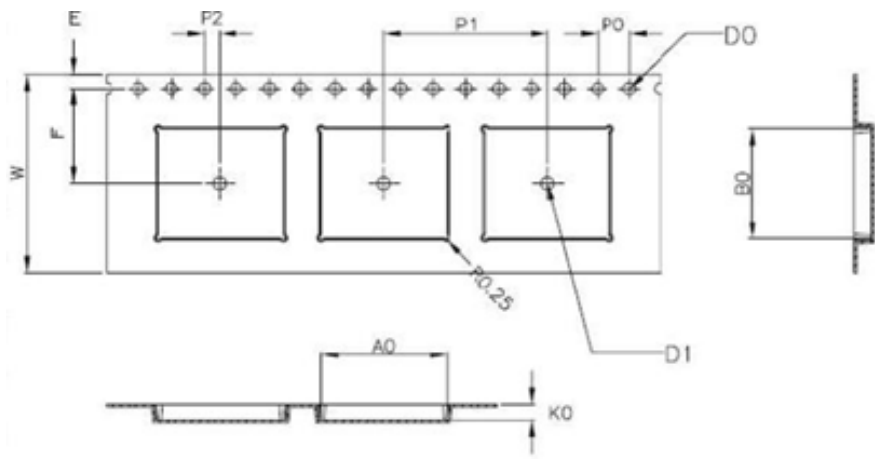
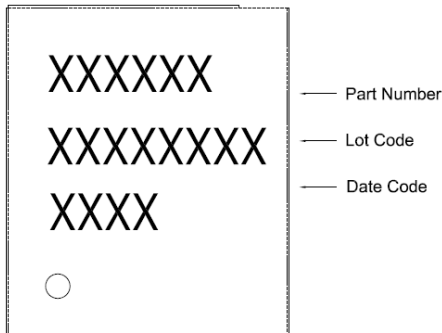
1. Referred to IPC/JEDEC standard
2. Peak Temperature: <260°C
3. Cycle of Reflow: 2 times max.
4. Adding Nitrogen (N₂) to implement 2000ppm or less of oxygen concentration during reflow process is recommended.
5. If the shelf time is exceeded, be sure baking step to remove the moisture from the component

9.1 Caution for SMT Preparation

Moisture Sensitivity Level: 4

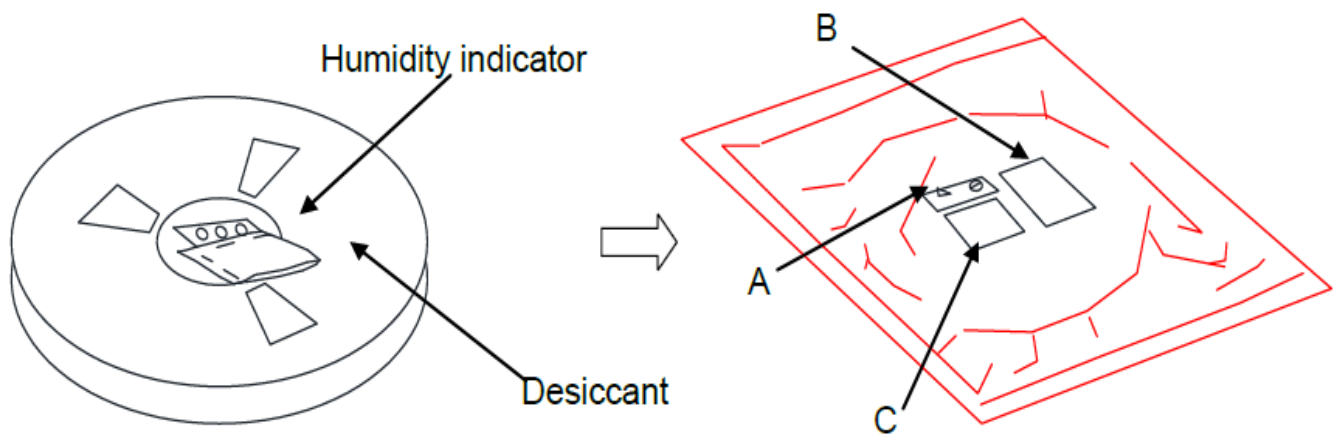
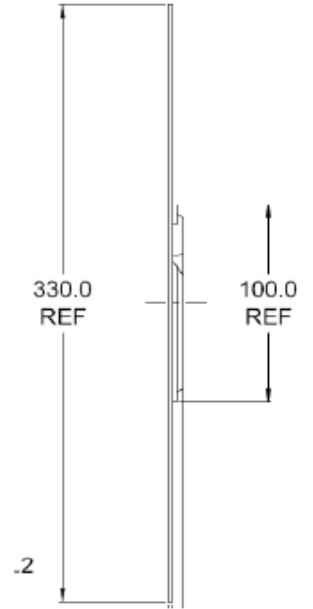
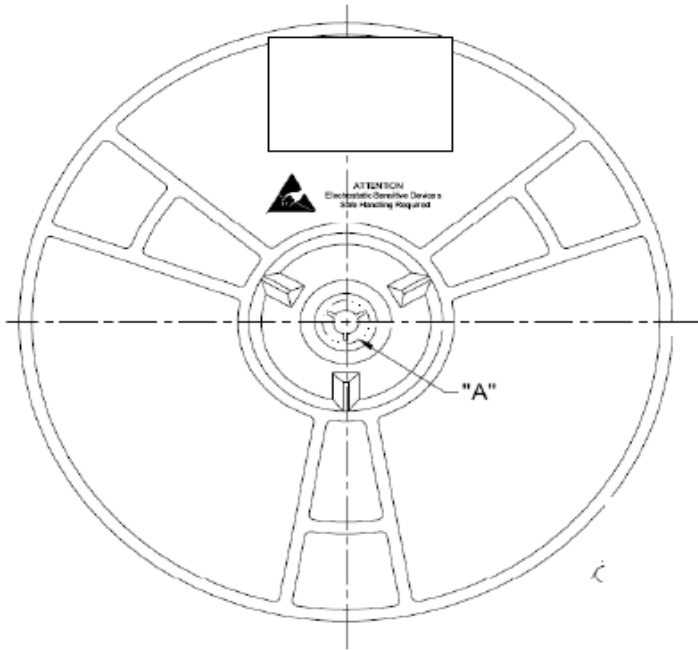
1. Calculated shelf life in sealed bag: 12 months at $<40^{\circ}\text{C}$ and $<90\%$ relative humidity (RH).
2. Peak package body temperature: 250°C .
3. After bag was opened, devices that will be subjected to reflow solder or other high temperature process must be
 - a) Mounted within: 72 hours of factory conditions $\leq 30^{\circ}\text{C}/60\%RH$ or
 - b) Stored per J-STD-033
4. Devices require bake before mounting, if:
 - a) Humidity Indicator Card reads $> 10\%$ for level 2a - 5a devices or $>60\%$ for level 2 devices when read at $23\pm 5^{\circ}\text{C}$
 - b) 3a or 3b are not met.
5. If baking is required, refer to IPC/JEDEC J-STD-033 for bake procedure.

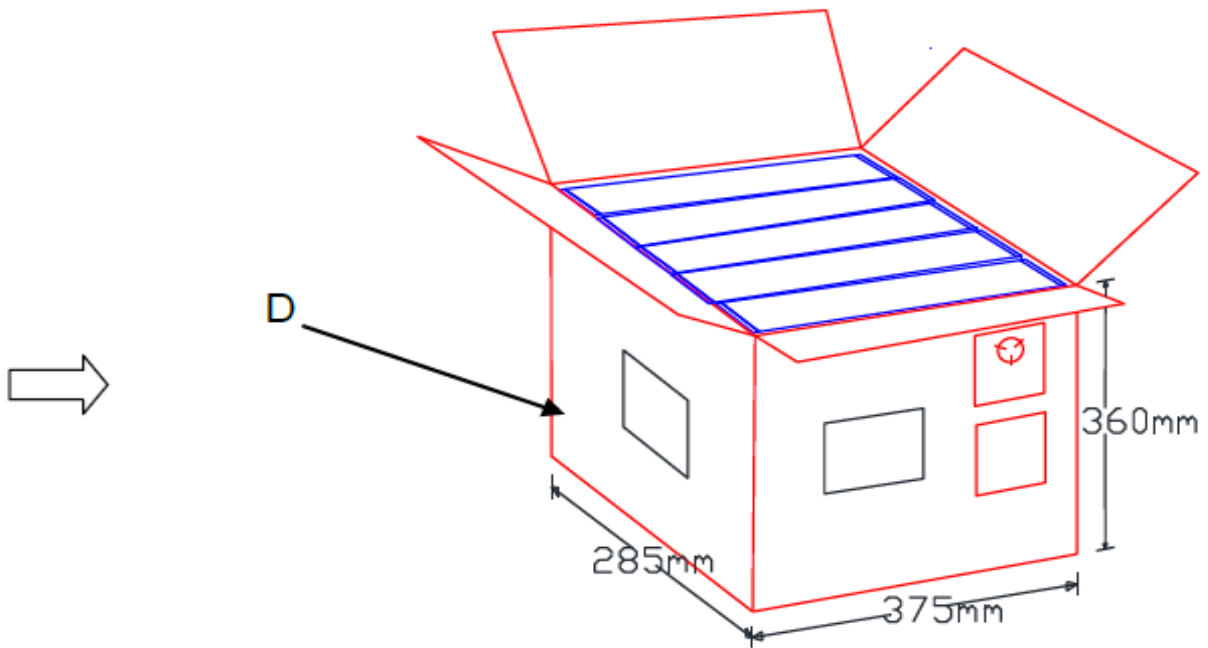
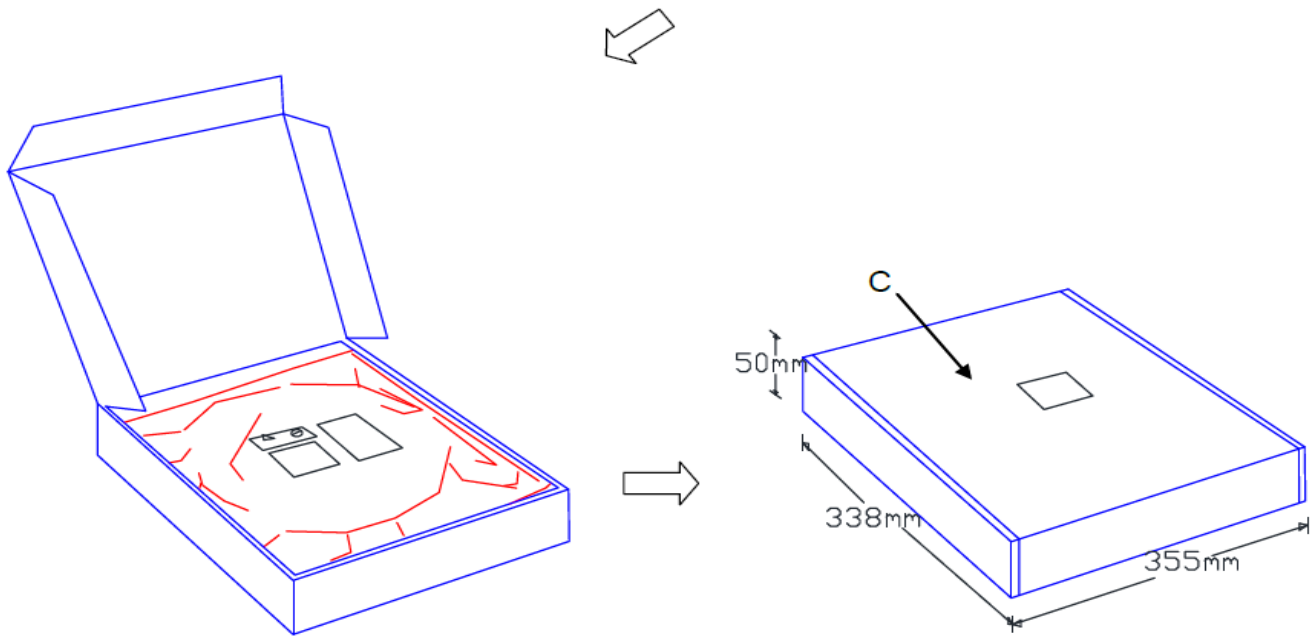
10. Package Information



W	24.00±0.30
A0	15.30±0.10
B0	13.30±0.10
K0	2.00±0.10
E	1.75±0.10
F	11.50±0.10
P0	4.00±0.10
P1	20.00±0.10
P2	2.00±0.10
D0	1.50 ^{+0.10} _{-0.00}
D1	∅ 1.50MIN

1. 10 sprocket hole pitch cumulative tolerance ± 0.20 .
2. Carrier camber is within 1 mm in 250 mm.
3. Material: Black Conductive Polystyrene Alloy.
4. All dimensions meet EIA-481-D requirements.
5. Thickness: 0.30 ± 0.05 mm.
6. Component load per 13" reel: 1000 pcs





Note: 1 tape reel = 1 box = 1,000pcs
1 Carton = 5 box = 5,000pcs

11. Ordering Information

Product Name	Part Number	Description
AP6281	TBD	11ax/ac/a/b/g/n 1T1R WiFi + BT5.2 Combo Sip Module